ISSN (Online) : 2319 - 8753
ISSN (Print) : 2347 - 6710

International Journal of Innovative Research in Science, Engineering and Technology

Volume 3, Special Issue 3, March 2014

2014 International Conference on Innovations in Engineering and Technology (ICIET'14)
On 21st & 22nd March Organized by

K.L.N. College of Engineering, Madurai, Tamil Nadu, India

Hybrid Modulation Switching Strategy for Grid Connected Photovoltaic Systems

Brindha.P[#1], Kaliamoorthy.M[*2], Arul prasanna.M[^3], Rajasekaran.V[$4]

[#1] PG Scholar, M.E– Power Electronics & Drive, PSNA College of Engineering & Technology, Dindigul, India.

[*2] Associate Professor, Department of EEE, Member IEEE, PSNA College of Engineering & Technology, Dindigul, India.

[^3] Assistant Professor, M.E– Department of EEE, Member IEEE, PSNA College of Engineering & Technology, Dindigul, India.

[$4] Professor, M.E – Department of EEE, Member IEEE,PSNA College of Engineering & Technology, Dindigul, India.

ABSTRACT— This work presents a novel single phase cascaded H-bridge multilevel inverter with least number of switches and isolated DC sources. The proposed inverter consists of two H-bridges connected in cascade. The upper H-bridge consists of five power electronic switches, capable of developing five level output and the lower H-bridge is capable of developing multilevel output. The conventional CHB inverter is replaced with the additional bi-directional switches in each cell. The proposed inverter consists of two H-bridges, the upper H-bridge is replaced with the addition of one bi-directional switch and the lower H-bridge is replaced with the bi-directional switches driven by hybrid modulation switching strategy. The upper inverter is switched at high frequency and the lower inverter is switched at low frequency. Hybrid modulation switching strategy is used to generate the multilevel output for the proposed inverter. The proposed inverter will be compared with the existing multilevel topologies on the basis of number of components, number of isolated DC sources, Switching losses and converter losses. The proposed inverter will be connected to the grid by proper synchronization along with maximum power point tracking algorithm. The proposed grid connected multilevel inverter will be simulated using MATLAB/SIMULINK and will be implemented in hardware using SPATRAN3A DSP.

KEYWORDS— Cascaded inverters, Hybrid modulation, maximum power point tracking, Bi-directional switch.

I. INTRODUCTION

Numerous industrial applications have begun to require higher power apparatus in recent years. For a medium voltage grid, it is troublesome to connect only one power
Semiconductor switch directly. As a result, a multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations. A multilevel converter not only achieves high power ratings, but also enables the use of renewable energy sources. Renewable energy sources such as photovoltaic, wind, and fuel cells can be easily interfaced to a multilevel converter system for high power applications [1].

Over the past few years, technological advances in power electronics and increasing demand for energy have contributed to rapid development of power generation based on renewable energy sources. Photovoltaic (PV), Wind and Fuel cell (FC) based renewable energy technologies have attracted the attention of researchers over the globe. One of the problems focused in the research is the constraint of power electronic switches. If the power electronic devices which can prolong high voltage are used in the inverter, their switching frequency is restricted. Hence, the device voltage must be reduced to use high-speed switching devices. A multilevel inverter can reduce the device voltage and the output harmonics by increasing the number of output voltage levels [15].

Further, increase in number of isolated DC sources in order to increase the number of output voltage levels leads to additional system complexity especially in PV and FC fed inverter topologies. The addition of isolated DC sources lead to the necessity of additional DC-DC converter, which are required to adjust the variable or low quality output voltage of the PV panels or FC stacks. Moreover power output of PV and FC stacks has to be maximized as it depends on the environmental condition. So in order to track the maximum power point of photo voltaic string or fuel cell stacks additional voltage and current sensors are required for each DC-DC converter. These additional sensors further increase the system complexity [6,7,8].

In single-phase multi-level inverters, the most widely used techniques are cascaded H-bridge (CHB), diode-clamped and capacitor-clamped types [8-11]. In addition, many other techniques also exist [12-20]. In particular, among these techniques, CHB single phase inverters have drawn attention because of their modularized circuit layout and simplicity [9]. Abundant modulation techniques and control paradigms have been developed for multilevel converters such as sinusoidal pulse width modulation (SPWM), selective harmonic elimination (SHE-PWM), space vector modulation (SVM), and others. In this thesis sinusoidal pulse width modulation (SPWM) is used [15].By increasing the number of cascaded H-bridges, the number of levels in CHB inverters increases. Generally if the number of output voltage levels is increased, then the number of power electronic devices and the number of isolated DC sources is also increased. This makes a CHB inverter further complex.

In this paper, a novel multilevel inverter with minimum number of power electronic switching devices is proposed which is a modified version of the multilevel inverter using series/parallel conversion of DC sources (MLISPC) developed in [17]. In the proposed multilevel inverter, an auxiliary circuit comprising of four diodes and a switch is introduced instead of series/parallel switches of the inverter found in MLISPC. However, only two isolated voltage sources is needed to output the same number of voltage levels compared to conventional CHB [1,4,5] inverters and MLISPC. In the proposed multilevel inverter, an auxiliary circuit comprising of four diodes and a switch is introduced instead of series/parallel switches of the inverter found in MLISPC. However, only two isolated voltage sources is needed to output the same number of voltage levels compared to conventional CHB inverters and MLISPC.

Section II describes the circuit topology of the proposed multilevel inverter, comparison of the proposed topology with other topologies are discussed. . In Section III describes the hybrid modulation switching strategy. In Section IV, converter losses are discussed. In Section V, and VI, validate the simulation results.

II. CIRCUIT TOPOLOGY

A. Overall System Structure

Fig.1 shows the block diagram of overall system structure, in which the PV string is connected to the DC-DC Boost Converter which tracks the sun to produce maximum power output from the solar array. Since the main application of the proposed inverter is fed from Photovoltaic (PV) array or Fuel cell (FC) stacks, DC-DC boost converters are required to boost the low output voltage of the PV panels or FC stacks. Hence here two boost converters are used one for the upper H bridge inverter and another for the lower H bridge inverter.

Hence, the DC-DC Boost Converter acts a maximum power point tracker. DC-DC Boost converters are used for two purposes they are,

1. For boosting low output voltage of PV array or FC stacks to desired value.
2. Balancing of DC link capacitors.

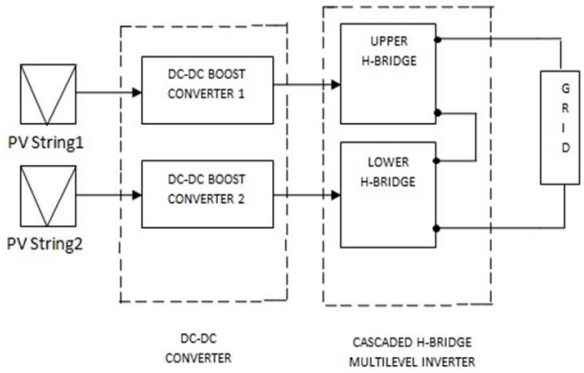


Fig.1: Block Diagram of overall system

The DC-DC Boost Converter feds the power to the proposed novel single phase cascaded H-bridge multilevel inverter with least number of switches. The proposed inverter consists of two H-bridges connected in cascade. Here the solar array acts as a isolated DC source which drives the inverter circuit. The upper H-bridge consists of five power electronic switches, capable of developing five level output and the lower H-bridge is capable of developing multilevel output. The upper inverter is switched at high frequency and the lower inverter is switched at low frequency. The outputs from the inverter are fed to the grid by proper synchronization. The efficient design of inverter circuit allows feed the voltage depending upon the requirement of grid voltage.

B. Proposed Cascaded H Bridge Multilevel Inverter Structure

Fig.2 shows the circuit configuration of the proposed inverter with two H bridge inverters

connected in cascade (Upper and lower H bridge inverters), where the inverter is driven by the hybrid modulation (HM) method. DC voltage sources V_{dc0} - V_{dcn} may either be independent or dependent on each other. Here the magnitude of each voltage sources in the lower H bridge is two times the magnitude of upper H bridge voltage source (i.e.,V_{dcn} = 2 V_{dc0}). The upper H-bridge is replaced with the one bi-directional switch and the lower H bridge of MLISPC is replaced with the bi-directional switches compared with the existing MLISPC.

Table I: Switching States of Lower H Bridge Inverter

Main Switches				**Auxiliary Switches**		**V_{dc}**
S5	S6	S7	S8	AS1	AS2	
1	0	0	1	1	1	3 V_{dc}
1	0	0	1	0	0	2 V_{dc}
1	1	0	0	0	0	V_{dc}
1	1	0	0	0	0	0
0	0	1	1	0	0	- V_{dc}
0	1	1	0	0	0	-2 V_{dc}
0	1	1	0	1	1	-3 V_{dc}

As shown in Fig.2, in the upper H-bridge, an auxiliary circuit comprising of four diodes and a switch is placed between two DC sources and the lower H bridge, auxiliary circuit comprising of two bi-directional switches which is placed in between separates the DC sources.

Using this proposed circuit configuration, the upper H bridge inverter separately can outputs, V_{up} as five levels, while the lower H bridge inverter separately can outputs, V_{low} as multilevel at its output because of increased number of bi-directional switches. Addition of one bi-directional switch increases the output level by four. In the proposed inverter structure the lower H-bridge inverter uses two bi-directional switches. The proposed inverter structure can outputs seventeen levels by combining the voltage levels V_{up} + V_{low} or V_{up} - V_{low}.

C. Comparison of Different Topologies of MLI

When the traditional CHB inverter is driven by the Hybrid Modulation method 16 switching devices are needed for 15 levels with the ratio of V_{dc0} : V_{dc1} :V_{dc2} :V_{dc3} = 1:2:2:2. But in case of proposed inverter it requires only 11 switching devices with the ratio of V_{dc0} : V_{dc1} :V_{dc2} :V_{dc3} = 1:2:2:2.On the other hand, in order to produce 11 levels at the output whereas, MLISPC topology requires 11 switching devices and 2 DC sources In addition, to increase the level further by four, MLISPC requires an addition of three power electronic devices and one additional DC source.

In the case of proposed inverter, it requires only 9 devices and 2capacitor sources for 11 levels at the load voltage and 11 switching devices and 3 capacitor sources for 17 levels. Therefore ,when the output level increase, the difference between the required number of switching devices for the proposed inverter decreases drastically when compared with that of the conventional CHB inverters and MLISPC inverter.

The proposed inverter can be smaller in size than the other two inverters because the number of switching devices is reduced significantly. Switching state of the lower H-bridge is shown in Table I.

Table II gives the component level comparison of different topologies of MLI.Table III gives the complete switching states and the derived output of the proposed multilevel inverter to generate 17levels.

Generally in the case of the asymmetrical cascaded H bridge inverters, it is possible to change the value of DC link or balancing capacitor voltage and sacrifice the redundancy in order to improve the quality of power by increasing the number of output voltage levels. Since in the proposed inverter, there exists only very little redundancy, balancing of capacitor voltages arises. Anyhow, the solution to the capacitor voltage balancing with reduced redundant levels is addressed in [15].

Table II: Comparison of Different Topologies of MLI

Topology	**Primary Devices(PD)**
Proposed Inverter	PD_{17}=11 for 17 levels
MLISPC	PD_{17} = 17 for 17 levels
Conventional CHB Inverter	PD_{17} = 18 for 17 levels

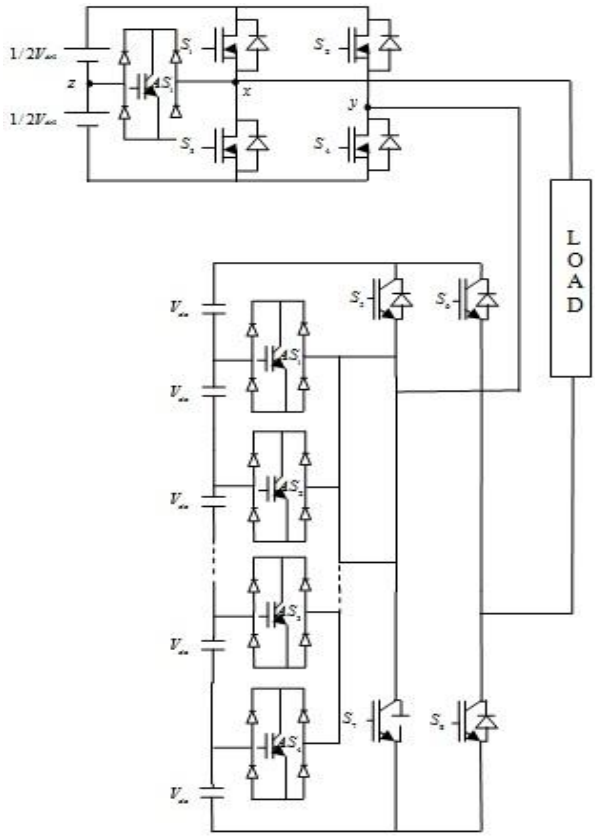


Fig. 2: Proposed Cascaded H-Bridge Multilevel Inverter.

III. HYBRID MODULATION SWITCHING TECHNIQUE

This section describes the determination of switching function for getting output of seventeen levels in the proposed inverter. The same procedure can be extended to drive the switching function for N level inverter. A hybrid PWM modulation technique was used to generate the PWM switching signals. Hybrid modulation switching strategy is a combination of fundamental frequency modulation (FPWM) and Multi-level Sinusoidal Pulse width modulation (MSPWM) for each inverter operation, so that the output inherits the features of switching-loss reduction from FPWM, and good harmonic performance from MSPWM. The power loss is the sum of switching and conduction losses. Hence, the proposed modulation technique yields the inverter to operate with reduced power loss across the switching devices. The well-known MSPWM scheme such as Single Carrier Sinusoidal Pulse Width Modulation (SCSPWM) is employed to generate the switching pulses. Compared to conventional MSPWM schemes, less number of commutations and considerable switching-loss reduction is obtained by using this modulation scheme.In this modulation technique, the upper bridge switches are commutated at FPWM, while the lower H-bridge switches are modulated at MSPWM, therefore the resultant switching patterns are the same as those obtained with MSPWM. A sequential switching scheme is embedded with this hybrid modulation in order to overcome unequal switching losses, and therefore, differential heating among the power devices.

Table III: Switching States of Proposed Inverter Structure

Main Switches		**Auxiliary Switches**		**V_{out}**
Upper Bridge	Lower Bridge	Upper Bridge	Lower Bridge	
S1,S4	S5,S8	-	-	4 V_{dc}
S4	S5,S8	AS1	-	3.5V_{dc}
S1,S4	S5,S8	-	-	3 V_{dc}
S4	S5,S8	-	AS1,AS2	2.5V_{dc}
S1,S2	S5,S8	-	AS1,AS2	2 V_{dc}
S4	S8	AS1	AS2	1.5 V_{dc}
S3,S4	S8	-	AS2	1 V_{dc}
S1,S4	S5,S6	-	-	0.5V_{dc}
S1,S2	S5,S6	-	-	0 V_{dc}
S3,S2	S7,S8	-	-	-0.5V_{dc}
S1,S2	S6	-	AS2	-1 V_{dc}
S2	S6	AS1	AS2	-1.5 V_{dc}
S3,S4	S7,S6	-	AS1,AS2	-2 V_{dc}
S2	S7,S6	-	AS1,AS2	-2.5V_{dc}
S3,S2	S7,S6	-	-	-3 V_{dc}
S2	S7,S6	AS1	-	-3.5V_{dc}
S3,S2	S7,S6	-	-	-4 V_{dc}

Fig.3. shows the voltage waveform when the proposed is driven by modulation method. The reference waveform is made by cutting on the amplitude of the carrier waveform. The modulation index M is defined as,

$$M_a = \frac{A_{e0}}{MA_{es}} \quad (1)$$

Where, $M = \frac{N-1}{2}$, N=11,15,17,19,23,…etc.,

Where A_{eo} and A_{es} mean amplitudes of the reference and carrier waveforms respectively. Main switches of the lower H-bridge inverter are switched as per the combination of modulated waveforms obtained from the upper H-bridge.

By combining the voltage waveforms generated from the upper and the lower bridges the output voltage waveform can be generated. Auxiliary switch is switched as per the modulation algorithm. The proposed PWM generation technique provides the generalized algorithm for any level of multi-level inverter circuit. Hence, in the proposed inverter structure the PWM generation will be simple if the levels are increased.

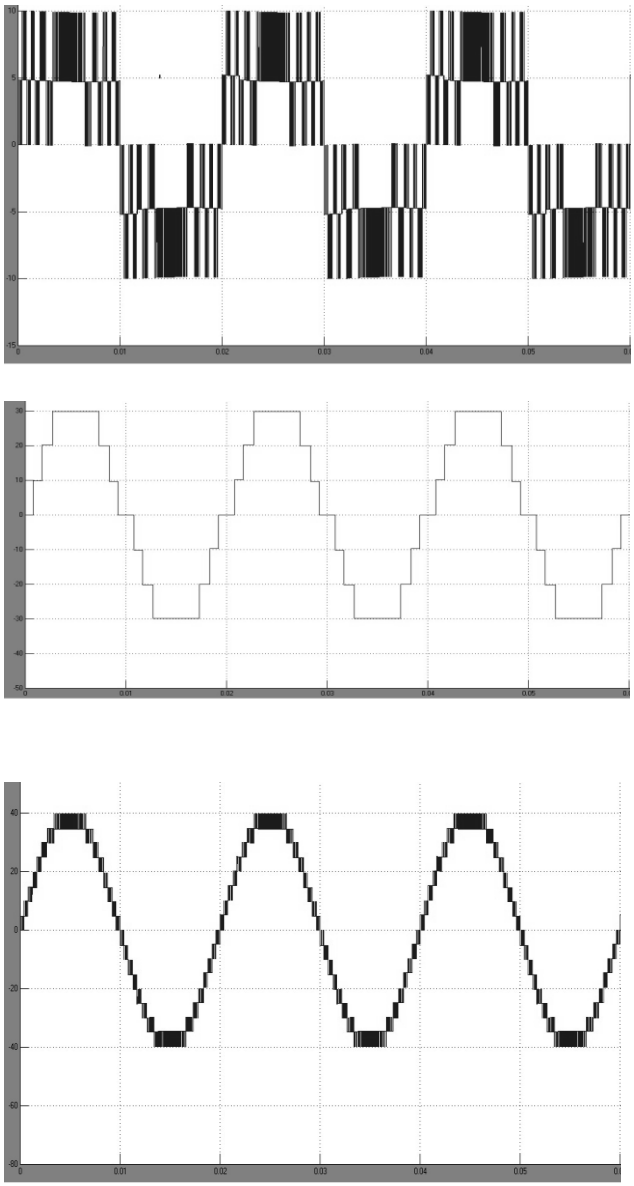
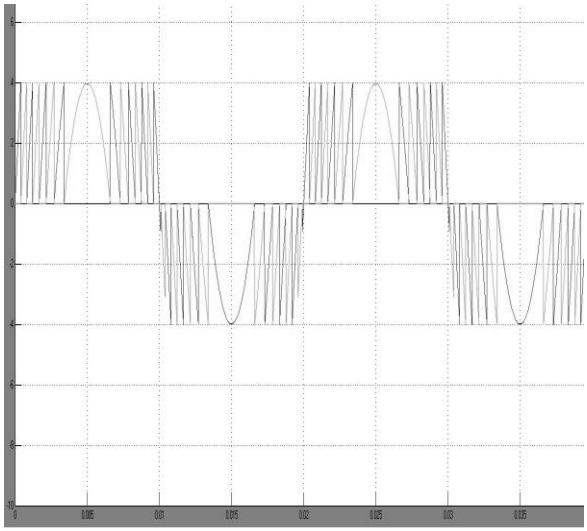
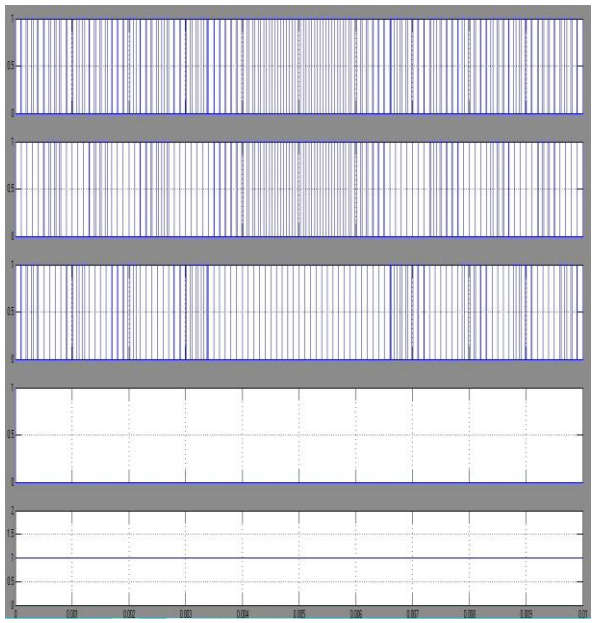


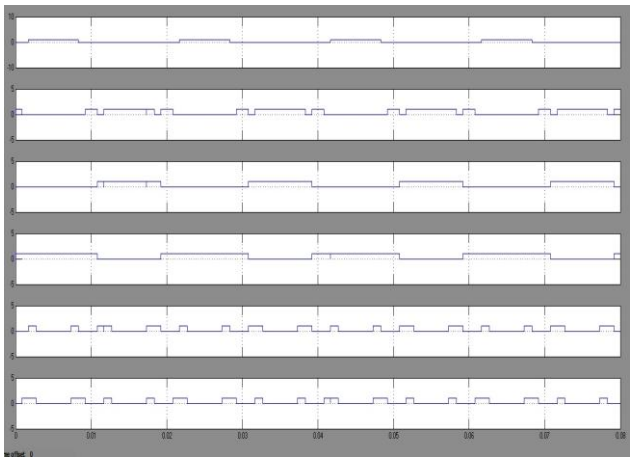
Fig.3. Voltage waveform of Upper Inverter, Voltage waveform of Lower Inverter, Total Voltage Waveform

IV. THD ANALYSIS

Hybrid modulation switching strategy is a combination of fundamental frequency modulation (FPWM) and Multi-level Sinusoidal Pulse width modulation (MSPWM) for each inverter operation, so that the output inherits the features of switching-loss reduction from FPWM, and good harmonic performance from MSPWM. The power loss is the sum of switching and conduction losses. Hence, the proposed modulation technique yields the inverter to operate with reduced power loss across the switching devices. As a result total harmonic distortion (THD) will be minimized. The well-known MSPWM scheme such as Single Carrier Sinusoidal Pulse Width Modulation (SCSPWM) is employed to generate the switching pulses for the upper H-bridge inverter switches. And the generalized switching algorithm can be implemented by combining the lower and upper switching pulses. The reference waveform for the upper inverter is modulated based on the voltage obtained by switching the lower inverter. Hence by changing the switching pattern of lower inverter the upper inverter wave shape can be adjusted to any required number of levels. The increased number of levels results the pure sinusoidal waveform as output.







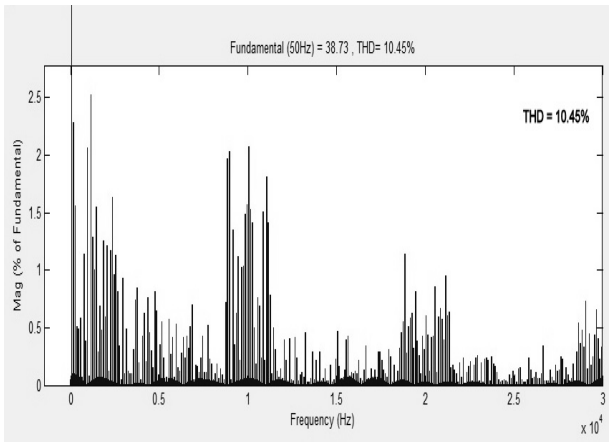


Fig.4. Modulated Reference voltage waveform of Upper Inverter, Gate Pulses for the Upper and Lower Bridges, THD waveform for Proposed Inverter.

V. SIMULATION RESULTS

The Above Cascaded Multi-level Inverter is simulated by using MATLAB/SIMULINK software tools for generating the 17 Level output voltage. This simulation is carried out for each cells in the proposed Inverter and the combined result is taken as the total output voltage.

To validate the proposed inverter topology simulation has been carried out for the proposed inverter in MATLAB/SIMULINK. The PWM modulation strategy discussed in section III was implemented in the simulation up to 17 levels and the same can be extended to any required level.

THD can be minimized by varying the modulation index of the proposed inverter. Switching stress can be minimized by proper switching of power electronic switches.

Table I gives the switching strategies for lower H bridge inverter and Table III gives the overall switching strategies for each and every cells in the proposed inverter. The upper inverter is operated at high switching frequency that is equivalent to the carrier frequency while the lower inverter is operated at low frequency (nearly equal to the fundamental frequency i.e. 50Hz).

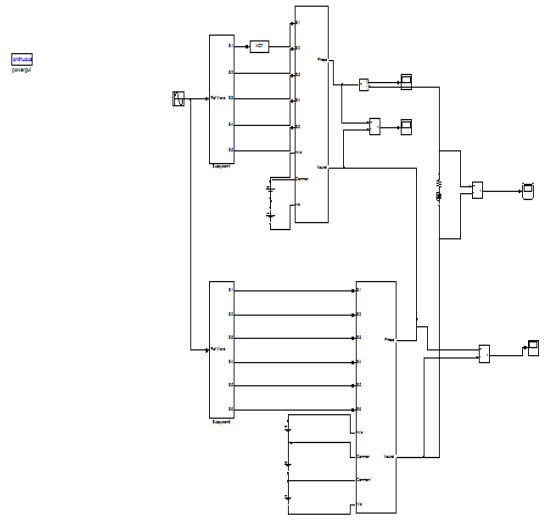


Fig.5. MATLAB Simulation Diagram- Proposed Cascaded H-Bridge Multi-Level Inverter

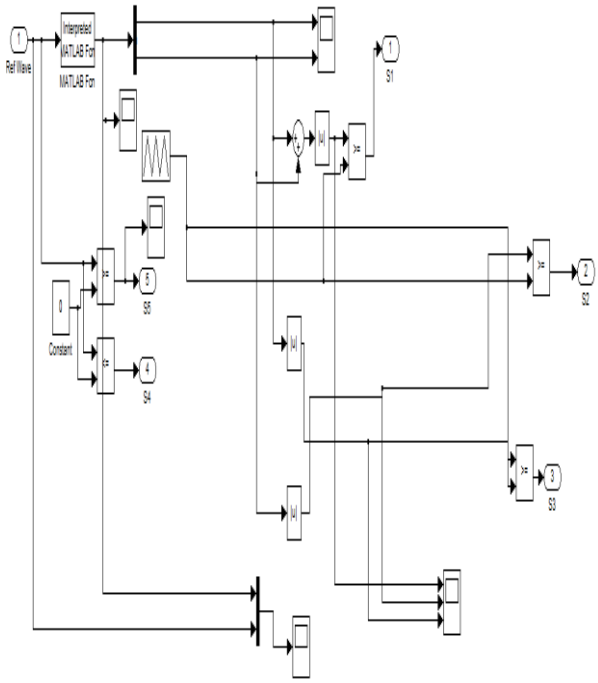


Fig.6. Reference wave signal generation for the upper bridge Inverter.

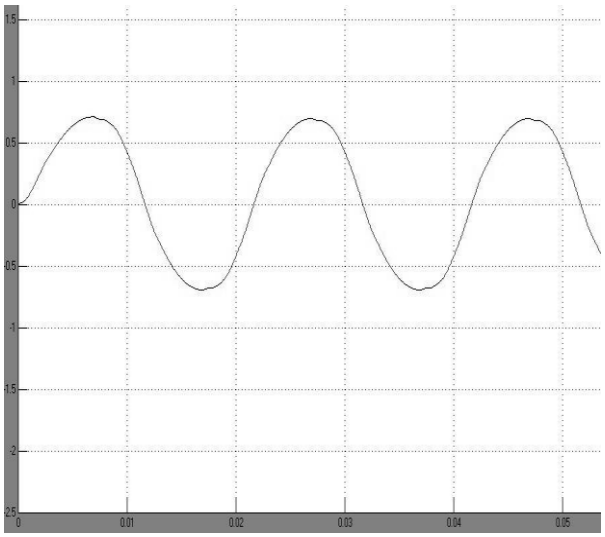


Fig.7. Output current waveform for the Proposed Inverter.

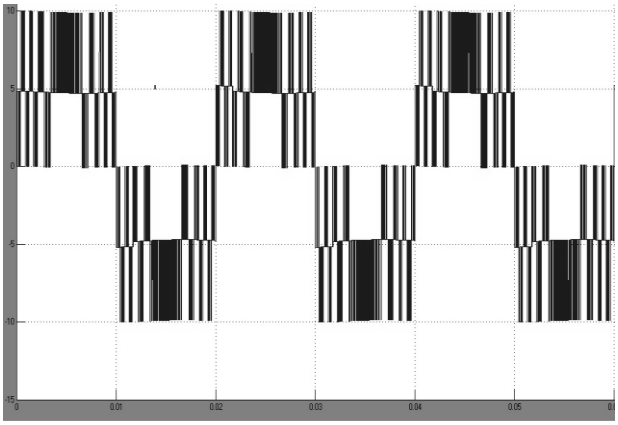


Fig.8. Output voltage waveform for the upper H-bridge Inverter.

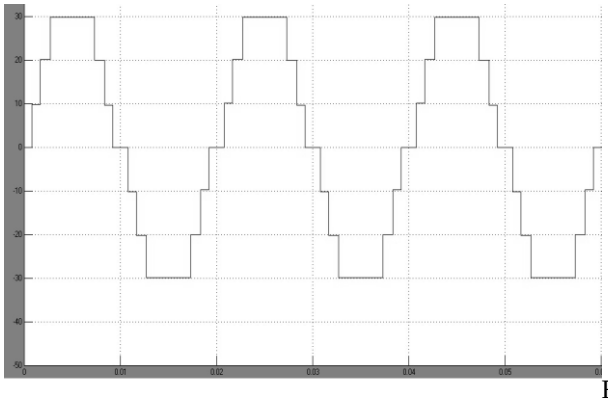


Fig.9. Output voltage waveform for the lower H-bridge Inverter.

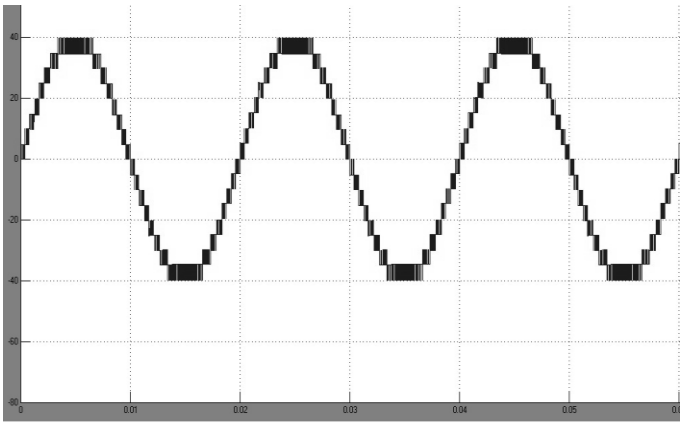


Fig.10. Output voltage waveform for the proposed Inverter.

VI. CONCLUSION

This paper has presents a novel single phase cascaded H-bridge Inverter with reduced number of power electronics devices and isolated DC sources. Simulations are carried out in MATLAB/Simulink. A Generalized switching algorithm which can be used for any number of levels is presented. The performance of the suggested novel cascaded H-Bridge multilevel inverter is investigated in detail. The modulation waveform and the harmonic analysis are also presented for various values of modulation strategies. By properly adjusting the modulation index, the required number of levels of the inverter output voltage can be achieved. This proposed inverter system offers the advantage of reduced switching devices and isolated DC sources when compared to the conventional CHB and MLISPC for the same number of output levels. Also, high frequency switching devices are operated at low voltage and low frequency devices are operated at high voltage. Thus it can be concluded that the proposed novel Cascaded H-Bridge Multilevel inverter can be used for medium and high power applications. The simulation results will be verified experimentally using SPATRAN3A DSP.

REFERENCES

[1] J. Rodriguez, J. S. Lai and F. Z. Peng, "Multilevel Inverters: Survey of Topologies, Controls, and Applications," IEEE Transactions on Industry Applications, vol. 49, no. 4, Aug. 2002, pp. 724-738.

[2] J. S. Lai and F. Z. Peng, "Multilevel Converters-A new Breed of Power Converters," IEEE Trans. Ind. Application., vol.32,pp. 509-517, May/June 1996.

[3] L. M. Tolbert, F. Z. Peng, and T. Habetler, "Multilevel Converters for Large Electric drives," IEEE Trans. Ind. Applicat.,vol.35,pp. 36-44, Jan./Feb. 1999.

[4] R. H. Baker and L. H. Bannister, "Electric Power Converter," U.S. Patent 3 867 643, Feb. 1975.

[5] A. Nabae, I. Takahashi, and H. Akagi, "A New Neutral-point Clamped PWM inverter," IEEE Trans. Ind. Application., vol. IA-17, pp. 518-523, Sept./Oct. 1981.

[6] R. H. Baker, "Bridge Converter Circuit," U.S. Patent 4 270 163, May 1981.

[7] P. W. Hammond, "Medium Voltage PWM Drive and Method," U.S. Patent 5 625 545, Apr. 1977.

[8] F. Z. Peng and J. S. Lai, "Multilevel Cascade Voltage-source Inverter with Separate DC source," U.S. Patent 5 642 275, June 24, 1997.
[9] P. W. Hammond, "Four-quadrant AC-AC Drive and Method," U.S. Patent 6 166 513, Dec. 2000.
[10] M. F. Aiello, P. W. Hammond, and M. Rastogi, "Modular Multi-level Adjustable Supply with Series Connected Active Inputs," U.S. Patent 6 236 580, May 2001.
[11] J. P. Lavieville, P. Carrere, and T. Meynard, "Electronic Circuit for Converting Electrical Energy and a Power Supply Installation Making Use Thereof," U.S. Patent 5 668 711, Sept. 1997.
[12] Meynard, J.-P. Lavieville, P. Carrere, J. Gonzalez, and O. Bethoux, "Electronic Circuit for Converting Electrical Energy," U.S. Patent 5 706 188, Jan. 1998.
[13] L. M. Tolbert, F. Z. Peng, and T. G. Habetler "Multilevel Converters for Large Electric Drives," IEEE Transactions on Industry Applications, vol. 35, no. 1, Jan/Feb. 1999, pp. 36-44.
[14] E. Cengelci, S. U. Sulistijo, B. O. Woom, P. Enjeti, R. Teodorescu, and F. Blaabjerg, "A New Medium Voltage PWM Inverter Topology for Adjustable Speed Drives," in Conf. Rec. IEEE-IAS Annu. Meeting, St. Louis, MO, Oct. 1998, pp. 1416
[15] C. GovindarajuAnd K. Baskaran, "Efficient Sequential Switching Hybrid-Modulation Techniques For Cascaded Multilevel Inverters", IEEE Transactions On Power Electronics, Vol. 26, No. 6, June 2011.
[16] Nasrudin A. Rahim, KrismadinataChaniago, and JeyrajSelvaraj "Single-Phase Seven-Level Grid-Connected Inverter for Photovoltaic System "IEEE Transactions On Industrial Electronics, Vol. 58, No. 6, June 2011.
[17] YouheiHinago and Hirotaka Koizumi "A Single-Phase Multilevel Inverter Using Switched Series/Parallel DC Voltage Sources," IEEE Transactions On Industrial Electronics, Vol. 57, No. 8, August 2010

BIOGRAPHY

Brindha.P has obtained her B.E degree in Electrical and Electronics Engineering from Bannari Amman University, Erode in the year 2011 and Pursuing her M.E., degree in Power Electronics and Drives Engineering from Anna University Chennai, during the year 2012- 2014. She has published 1 paper in International Conference. Her area of interest includes Power Electronics, Renewable Energy Systems and Electrical Machines. She has 1.4 year of working experience as Application Developer in iNautix Technologies India pvt.,ltd.

Kaliamoorthy.M has obtained his B.E degree from Bharathiar University, in the year 1998 and M.E., degree from Anna University Chennai, in the year 2004. He has secured first rank in M.E and got gold medal. He had completed his Ph.D under Anna University Chennai, in the year 2014. He has published 13 papers in National Conferences and 4 papers in International Conferences. He has also published 5 papers in International journals. His areas of interest include Power Electronics, Control of Drives and Renewable Energy systems. He is a life member of ISTE. He has 13 years of teaching experience. Currently he is working as an Associate Professor in the department of Electrical and Electronics Engineering at PSNA College of Engineering and technology, Dindigul, Tamil Nadu, India.

Arul Prasanna.M was born in 18th May 1985. He has received his B.E., in Electrical and Electronics Engineering, M.E., in Power Electronics and Drives from Anna University, Chennai, TamilNadu and pursuing Ph.D., in Power Electronics and Drives Anna University, Chennai, TamilNadu. His research interest includes Power Electronics and Drives, Current Source Inverters, AC drives and application. Currently he is working as a Assistant Professor in Electrical and Electronics Engineering department at P.S.N.A College of Engineering and Technology, Dindigul, TamilNadu, India.

Rajasekaran.V was born in Madurai, Tamil Nadu, India in 1971. He received his BE (Electrical and Electronics Engg) in 1994, ME (Power Systems) in 1997, and PhD in 2007 from Madurai Kamaraj University, Madurai, India. He is now heading the Electrical and Electronics Department, PSNA CET, Dindigul, TamilNadu, India. He is a certified Energy auditor. His fields of interest are Power Systems, Energy, Power Quality, Power Electronics Energy etc.