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Implementation of High Speed MDC FFT/IFFT Processor for MIMO-OFDM Systems

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ABSTRACT: The architecture of multipath delay commutator (MDC) and memory scheduling are the basic concepts used to implement fast Fourier transform (FFT) processors with variable length. These FFT processors are used in orthogonal frequency division multiplexing systems, having multiple number of inputs and multiple number of outputs. Depending on this MDC architecture, we implement the fft/ifft processor based design which is proposed in this paper. In this design we implement ram, fifo, input buffer and output sorting buffer. The functionality verification and the synthesis is carried out using XILINX ISE 12.3i and shows the reduced delay values.

KEYWORDS: Fast Fourier Transform (FFT), memory scheduling, multiple-input and multiple-output (MIMO), orthogonal frequency division multiplexing (OFDM), output sorting, pipeline based multipath delay commutator (MDC), WiMAX.

I.INTRODUCTION

When we require a data to be encoded at multiple frequencies then the popular scheme generally used is orthogonal frequency division multiplexing. This type of scheme is famous at wideband digital communication. Whether it may be wired or wireless such as television, broadcasting of audio, internet accessing, wireless networks and is widely used in latest technology like 4G mobile communication. Digital multi carrier modulation technique is used for OFDM, When we require to carry parallel streaming of data, a large spaced orthogonal sub-carrier signals are used in which each sub-carrier undergo convolution modulation like quadrature amplitude modulation or phase shift keying. OFDM have capability of channel equalization because it uses slowly modulated narrow band signals instead of using one highly modulated wide band signal. Using OFDM, FFT can be implemented without loss in efficiency. Narrow band co channel interfacing becomes very robust using ofdm .it is very less sensitive over time synchronization errors. These type of OFDM signals have broad range of usage in WLAN under the standard of 802.11a,and digital radio systems standards like DAB/ERUKA 147,Terristial Digital TV systems(DVB-T)and Terrestrial Digital mobile systems(DVB-T)

Fast Fourier transform are used to compute discrete Fourier transform and also for its inverse .These technique used to convert to signals from time to frequency domain and vice versa.fft makes numeric algorithm as simple such that it is used in image processing and signal processing applications. In previous DFT is existed ,in which the fastness drawback has overcome by fft.Ofdm uses reverse fft and transmitter side and fft and the receiver side to perform modulation and demodulation efficiently. Fft with ofdm is used cpu like intel Pentium at 1.26GHZ frequency and is able to calculate a 8 192 fft with in 576µs using FFTW, and in cpu called intel Pentium M AT 1.6 GHZ frequency and able to within 387 µs. a compared to earlier generation cpu ,a wide range of fft-ofdm based cpu named intel core 2 duo which operates at3 Ghz frequency and able to perform the operations at 96.

MIMO-OFDM defines multi input and multi output orthogonal frequency division multiplexing which is dominated over 4G and 5G wireless communications. The word multi input and multi output defines which is capable of sending multiple signals over multi antennas and orthogonal frequency division multiple communication system without loss in reliability . In earlier mimo is used with a combination of time division multiple access ,code division multiple access ,but mimo with ofdm is much famous for its high data rate,high message deliver capacity ,high throughput .for these reasons only it is familiar at wires LAN and some standard networks at mobile communications . In mdc based mimo-ofdm as the data size increases the memory size also increases rapidly, but by using multipath delay commutator the

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data flow will be controlled in simplest manner. the main reason for implementing mimo based ofdm is for its simplicity and which makes the user data in to a closely spaced narrow sub channels in such to eliminates bigger obstacles to increase reliability.

II.LITERATURE SURVEY

FAST Fourier transform (FFT) is the major block in orthogonal frequency division multiplexing systems. Ofdm has allocated in a large range of applications from wired-communication modems, such as digital subscriber lines (xDSL) [1], [2], to wireless-communication modems, like IEEE802.11 [3] WiFi, IEEE802.16 [4], [5] WiMAX or 3GPP long term evolution (LTE), to process baseband data.

Inverse fast Fourier transform (IFFT) converts the modulated information from frequency domain to time domain for transmission of radio signals, while FFT gathers samples from the time domain, again converting them to the frequency domain.

Y.G.Li, J.H. Winters and N.R.Sollenberger[6] proposed multiple input multiple output (MIMO) devices, data throughput can be increased drastically. Hence MIMO-OFDM systems provide data rate and reliability in wireless communications. To handle “multiple” data streams, firstly the functional are to be duplicated for processing the given inputs. Without a proper design, the complexity of FFT/IFFT processors in MIMO systems increases linearly with the number of data streams.

B. G. Jo and M. H. Sunwoo [8] proposed pipelines schemes, are the architectures most widely adopted for the implementation of FFT/IFFT. From the memory access perspective, in-place memory updating schemes performs the computation in three phases: writing in the inputs, updating intermediate values, and reading out the results. In updating phase, the processor reuses the radix-*r* processor, such that a single radix-*r* butterfly is sufficient to complete *N*-point FFT/IFFT computation. Since each phase is non-overlapped, the outputs can be sequential or as requested. However, it is the non-overlapping characteristic that makes the butterfly idle in memory write and read phases, and the overall process is lengthy. Continuous-flow mixed radix (CFMR) FFT.

P. Y. Tsai and C. Y. Lin [9] utilizes two *N*-sample memories to generate a continuous output stream. One of the memories is used to calculate current FFT/IFFT symbols, while the other stores the previously computed results and controls the output sequence. Thus, when CFMR is used in MIMO systems, the required memory is increased in a trend proportional to $2\times Ns$, where *Ns* is the number of data streams. Such memory requirement may be forbidden if *Ns* is large, because the area of memory does not shrink as much as that of logic gates when fabrication technology advances, due to the use of sense amplify circuitry.

III.FFT/IFFT PROCESSORS

Fast Fourier Transform and Inverse Fast Fourier Transform are the most efficient and fast algorithms to calculate the Discrete Fourier Transform and Inverse Discrete Fourier Transform respectively. Fast Fourier Transform/Inverse Fast Fourier Transform is mostly used in many communication applications like Digital Signal Processing and the implementation of this is a growing research. From the last years, OFDM became an important one in FFT/IFFT algorithms and is going to be implemented. The efficient multiple access method for Bandwidth in digital communications is OFDM (Engels, 2002; Nee & Prasad, 2000). Many of nowadays OFDM technique can be used in most important wireless communication systems: Digital Audio Broadcasting (DAB) (World DAB Forum, n.d.), Digital Video Broadcasting (DVB) , Wireless Local Area Network (WLAN) , Wireless Metropolitan Area Network (WMAN) and Multi Band –OFDM Ultra Wide Band (MB–OFDM UWB). Moreover, this method is also utilised in important wired applications like Asymmetric Digital Subscriber Line (adsl) or Power Line Communication.

Every communication system must have both Transmitter and Receiver. At the Transmitter side, IFFT is used for modulating signal, which depends on the OFDM system and at the Receiver side, FFT is used for demodulating signal. The FFT/IFFT are the important modules in OFDM transceivers. From this we can say that, the most parts of OFDM systems are, IFFT can be used at the transmitter side where as viterbi decoder can be used at the receiver side

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(Maharatna et al., 2004). The FFT is the second calculative huge block at the receiver section. The fft and ifft must be implemented such that to achieve the required throughput with the reduced area and delay. The modern ofdm transceivers requirements may lead to the implementation of special hardware, which is the critical block in the transceiver. Hence the fft/ifft can be implemented as a Very Large Scale Integrated circuit. The methods that we applied to the FFT can also be applied to the IFFT. From the output of a FFT processor,we can easily get the ifft. Therefore, the discussion in this chapter concentrates on the FFT without loss of generality.

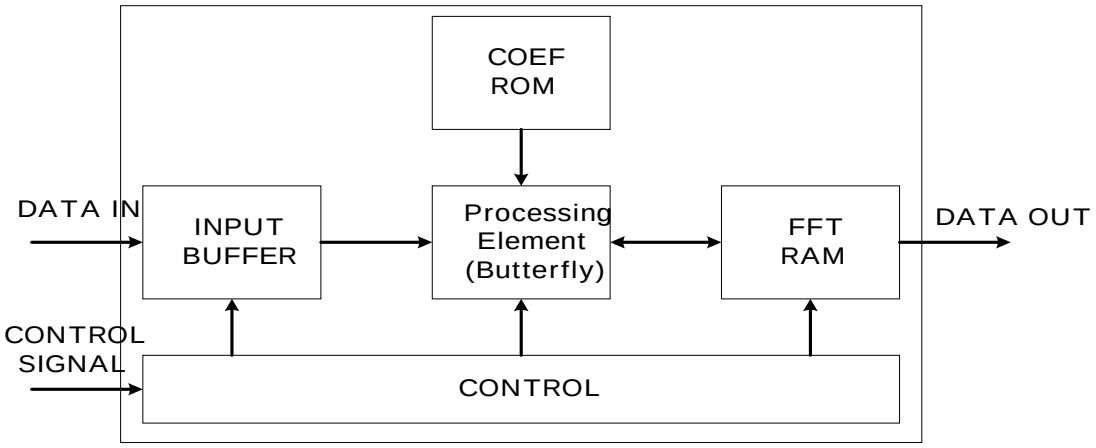

Figure1. Internal architecture of fft/ifft processors

The inverse discrete Fourier transform can be found using Which can be expressed as Where is called the twiddled factor We can see that the difference between the inverse discrete Fourier and forward Fourier transform is the twiddled factor and the division by 1/N is called the twiddled factor.

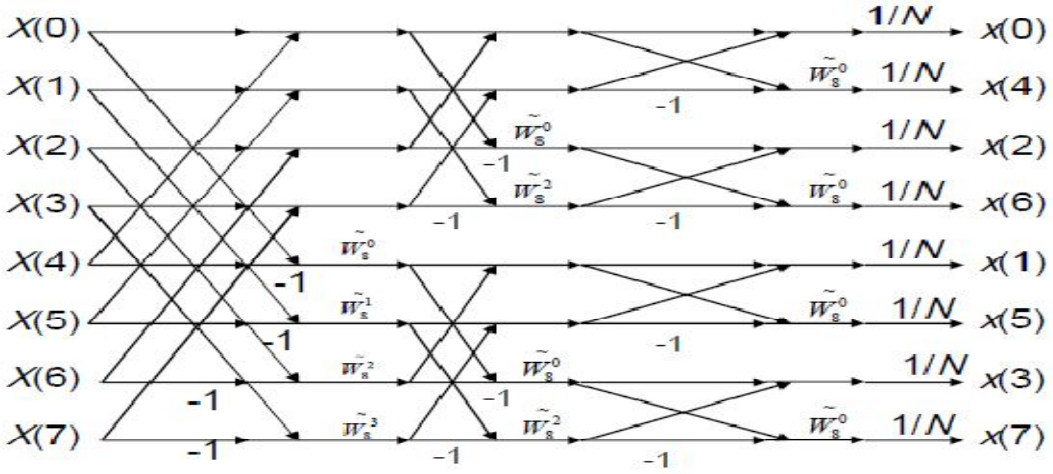

Figure 2. Inverse Fourier Transform

Wireless technologies have evolved remarkably since Guglielmo Marconi said that the ability of radio can provide good contact with the ships sailing in the English channel in 1894. New theories and applications of wireless technologies have been developed by hundreds and thousands of scientists and engineers through the world ever since.Wireless communications can be regarded as the most important development that has an extremely wide range of applications from TV remote control and cordless phones to cellular phones and satellite-based TV systems. It changed people's life style in every aspect. Especially during the last decade, the industry of mobile radio

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communication is growing exponentially with increasing rate, fueled by the digital and RF (radio frequency) circuits design, fabrication and integration techniques and more computing power in chips. This trend will continue with an even greater pace in the near future.

The advances and developments in the technique have partially helped to realize our dreams on fast and reliable communicating \any time anywhere". But we are expecting to have more experience in this wireless world such as wireless Internet surfing and interactive multimedia messaging so on. One natural question is: how can we put high-rate data streams over radio links to satisfy our needs? New wireless broadband access techniques are anticipated to answer this question. For example, the coming 3G (third generation) cellular technology can provide us with up to 2Mbps(bits per second) data service. But that still does not meet the data rate required by multimedia media communications like HDTV (high-definition television) and video conference. Recently MIMO-OFDM systems have gained considerable attentions from the leading industry companies and the active academic community.A collection of problems including channel measurements and modeling, channel estimation, synchronization, IQ (in phase-quadrature) imbalance and PAPR (peak-to-average power ratio) have been widely studied by researchers .Clearly all the performance improvement and capacity increase are based on accurate channel state information. Channel estimation plays a significant role for MIMO-OFDM systems. For this reason, it is part of my dissertation to work on channel estimation of MIMO-OFDM systems.

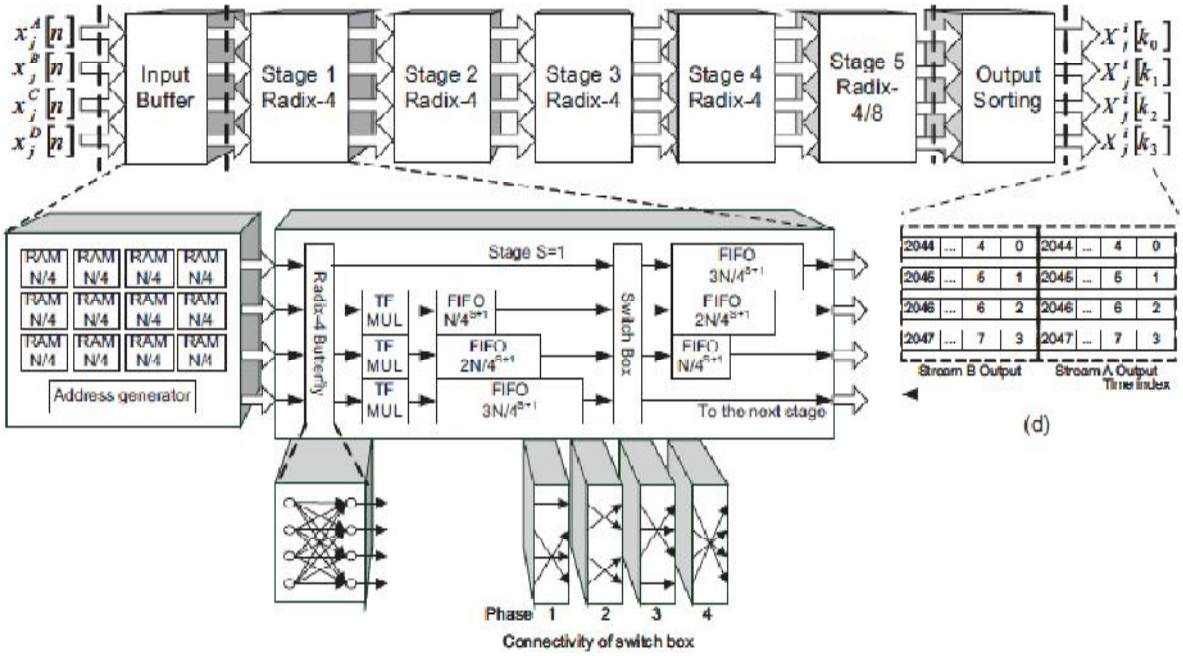

Figure 3. Proposed MIMO fft/ifft Processor

Multiple Input Multiple Output (MIMO) systems are devices that are used in wireless communication. These are devices consisting of array of transmitters and receivers. With MIMO device it is possible to obtain high data. Hence combination of MIMO and OFDM system provides efficient data rate and reliability in wireless communications. IEEE 802.16 WIMAX (Worldwide Interoperability for Microwave Access) is a wireless communications standard, which can provide a data rates from 30 to 40 megabit/sec. 3GPP (3rd Generation Partnership Project) is the recent evaluation in IEEE 802.16 WiMAX. The 3rd Generation Partnership Project initiative evolved from a strategic one, which is between Nortel Networks and AT&T Wireless. AT&T Wireless was worked with an IS-136 time division multiple access wireless network present in the United States in 1998.Nortel Networks Wireless, which is an R&D center in Richardson, which is a wireless division of Bell Northern Research and developed a new one for " Internet Protocol " wireless network and the internal name is "Cell Web".

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IV.FFT PROCESSOR INVOLVED METHODS

Fast Fourier Transform is an algorithm proposed by Cooley and Tukey to compute Discrete Fourier transform (DFT) which converts time to frequency and reduces the time complexity to O(N log 2N), where N denotes the size of FFT. When considering the other implementations, the FFT/IFFT algorithm is chosen such that the speed of execution, hardware complexity, flexibility and accuracy. But for real time systems, the speed of execution is the major thing. Based on this, Several architectures have been taken place from the last 300 years such as architecture having single and double memory, cached memory architecture, array based architecture, and pipeline based architecture for the purpose of hardware implementation, various FFT processors have been used mainly 2 types of architectures.

a. Memory based architecture
b. Pipeline based architecture

Memory based architecture cannot be parallelized where as the pipeline architecture can overcome the disadvantages of the former one. Pipeline based architectures worked in real time, continous processing and having smaller latency with less delay which is required for most of the applications.

Generally, the pipeline FFT processors are classified in two design- architectures.
a. Single-path delay feedback (SDF) pipeline architecture
b. Multiple-path delay Commutator (MDC) pipeline architecture.

Single path delay feedback (SDF) reduces amount of multipliers but it complicates the control mechanism and uses more memory resources whereas Multipath Delay Commutator saves more area,[5] and thus MDC is adopted as the hardware architecture. Multipath Delay Commutator (MDC) makes the feedback paths in to feed forward streams using switch boxes along with memory.In this paper Multipath Delay Commutator and memory scheduling are used to implement fast fourier transform in orthogonal frequency division system with variable length for multiple input and multiple output. From the above two things, we can say that the delay feedback is more efficient than delay commutator for the proper utilization of memory. For computation of FFT we need to use twiddle factor to multiply with input signals to obtain output, and for this a huge size of ROM is required to store twiddle factors which in turn increases the cost.

Thus for further improvement, ROM-less FFT/IFFT processor which eliminates ROM‟s that store twiddle factor is presented. The complex multipliers are used for this purpose and they perform shift-and-add operations, thus the processor uses a digital multiplier with 2 inputs and does not require any storage element like ROM, to store twiddle factor. Thus the proposed architecture also includes a reconfigurable complex constant multiplier to store twiddle factor instead of using ROM‟s.

V.RESULTS

A. RTL SCHEMATIC: This shows the inputs and outputs of the proposed system. Based on the clock and reset signals, the output data each of 32 bit is obtained.

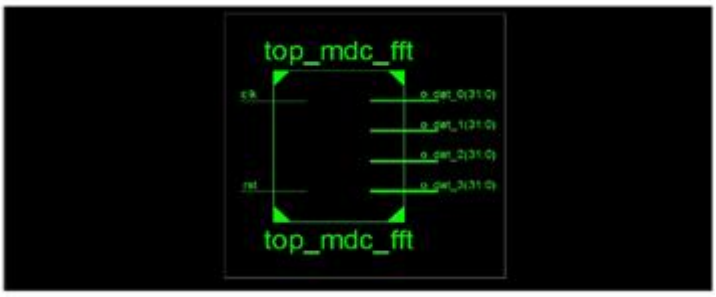

Figure4. RTL view of mdc fft/ifft processor

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B. SIMULATION RESULTS: This shows that the proposed system consist of output buffer having the sample data of 2048 samples, which are unsigned decimal.

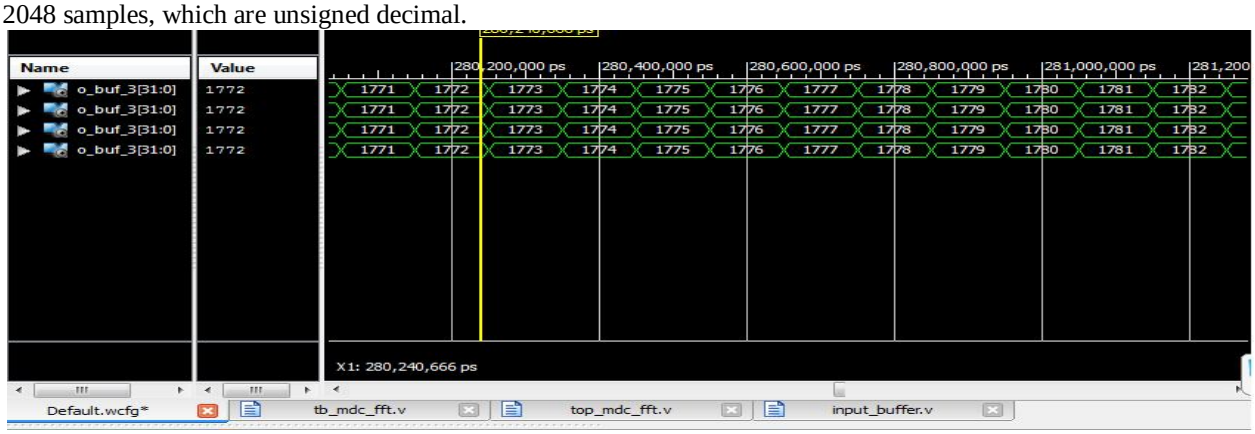
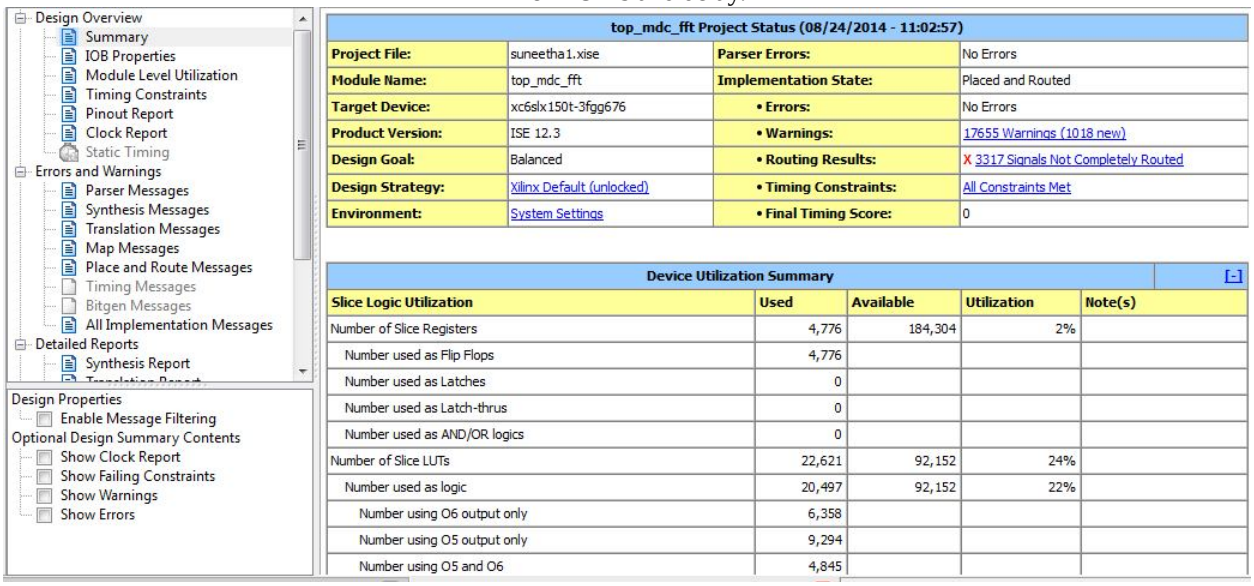


Figure5. Output Data

C. DESIGN SUMMARY: This shows that the proposed system consists of synthesis report, memory usage, Number of LUT's and delay.



top_mdc_fft Project Status (08/24/2014 - 11:02:57)			
Project File:	suneetha1.xise	**Parser Errors:**	No Errors
Module Name:	top_mdc_fft	**Implementation State:**	Placed and Routed
Target Device:	xc6slx150t-3fgg676	**• Errors:**	No Errors
Product Version:	ISE 12.3	**• Warnings:**	17655 Warnings (1018 new)
Design Goal:	Balanced	**• Routing Results:**	X 3317 Signals Not Completely Routed
Design Strategy:	Xilinx Default (unlocked)	**• Timing Constraints:**	All Constraints Met
Environment:	System Settings	**• Final Timing Score:**	0

Device Utilization Summary				[-]
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Registers	4,776	184,304	2%	
Number used as Flip Flops	4,776			
Number used as Latches	0			
Number used as Latch-thrus	0			
Number used as AND/OR logics	0			
Number of Slice LUTs	22,621	92,152	24%	
Number used as logic	20,497	92,152	22%	
Number using O6 output only	6,358			
Number using O5 output only	9,294			
Number using O5 and O6	4,845			

Figure6. Summary of the proposed mdc fft/ifft processor

VI. CONCLUSION

The proposed high speed MDC architecture and memory scheduling are very much suitable for FFT/IFFT processor in multiple input multiple output OFDM system, because the constant multipliers are used to store the twiddle factors instead of ROM, Which utilizes 100% area and reduces the delay.

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BIOGRAPHY

T.S. Ghouse Basha is presently working as an Associate Professor and HOD in the Department of Electronics and Communication Engineering in KORM College of Engineering, Kadapa. He carried out his MTech project work in Defence Research and Development Laboratory, Hyderabad and working in teaching field since eleven years in different cadres. He received his BTech and M.Tech from the Department of Electronics and Communication Engineering from JNTU University and Nagarjuna University respectively. He has submitted his Ph D thesis in microwave antennas to JNTUA. His areas of interest include microwave antennas, digital signal processing and mobile communications.

L.Suneetha pursuing M.Tech[VLSI] in KORMCE, Kadapa. She completed Bachelor of Technology from Annamacharya Institute of Technology and Sciences, Rajampet, Kadapa. Her areas of interest are Communications, Microprocessors and Microcontrollers, VHDL.