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Modified Multilevel Inverter Topology for Driving a Single Phase Induction Motor

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Abstract: The multilevel inverter utilization has been increased since the last decade. These new type of inverters are suitable in various high voltage & high power application due to their ability to synthesize waveforms with better harmonic spectrum and faithful output**.**. This paper presents a multilevel inverter configuration which is designed by insertion of a bidirectional switch between capacitive voltage sources and a conventional H-bridge module. The modified inverter can produce a better sinusoidal waveform by increasing the number of output voltage levels. By serial connection of two modified H-bridge modules, it is possible to produce 9 output voltage levels including zero. Multicarrier phase-shifted pulse-width modulation method is used to generate control signals. The analysis of the output voltage harmonics is carried out. From the results, the proposed inverter provides higher output quality with relatively lower power loss as compared to the other conventional inverters with the same output quality. Also the hardware implementation was made with induction motor load.

Keywords: Cascaded H-bridge multilevel inverter (CHB), phase shifted modulation, multicarrier pulse-width modulation, total harmonic distortion (THD).

I. INTRODUCTION

Over the past two decades, multilevel inverters have attracted wide interest both in the scientific community and in the industry. The reason for the increased interest is that the multilevel inverters are a viable technology to implement controlled rotational movement in high-power applications. Multilevel inverters include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms. The commutation of the switches permits the addition of the capacitor voltages, which reach high voltage at the output, while the power semiconductors must withstand only reduced voltages. Multilevel converters have a lot of advantages to offer in medium- to high-voltage range of applications. These include variable speed motor drives and power system applications. Multilevel converters can synthesize waveforms using more than two voltage levels, Small filter components are required and sometimes they can be left out altogether. Disadvantages of multilevel topologies include: high number of semiconductor devices, complex control as a result of the large number of controlled devices, large number of gate drive circuits, several DC voltage sources are required, need to balance voltages across capacitors used in voltage divider circuits. There are different types of multilevel circuits involved. The first topology introduced was the series H-bridge design. This was followed by the diode clamped converter, which utilized a bank of series capacitors. A later invention detailed the flying capacitor design in which the capacitors were floating rather than series-connected. Another multilevel design involves parallel connection of inverter phases through inter-phase reactors. In this design, the semiconductors block the entire dc voltage, but share the load current. Several combinational designs have also emerged some involving cascading the fundamental topologies. These designs can create higher power quality for a given number of semiconductor devices than the fundamental topologies alone due to a multiplying effect of the number of levels. The multilevel inverters are mainly classified as diode clamped, Flying capacitor inverter and cascaded multilevel inverter. The cascaded multilevel control method is very easy when compare to other multilevel inverter because it doesn't require any clamping diode and flying capacitor. In this paper, we are using a new topology of cascaded H-bridge multilevel inverter for producing nine output voltage levels and for that we are using multicarrier modulation technique. This paper is organized as follows: the inverter's configuration is presented in Section II, the PWM modulation strategy in Section III, analysis of output voltage and harmonics in Section IV, the hardware implementation in Section V and Section VI is the conclusion.

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II. .NINE-LEVEL CASCADED H-BRIDGE MULTILEVEL INVERTER

Cascaded multilevel inverter has the advantage of most reliable and to achieve the best fault tolerance owing to its modularity; a feature that enables the inverter to continue operating at lower power levels after cell failure. Modularity also permits the cascaded multilevel inverter to be stacked easily for high power and high voltage applications. The cascaded multilevel inverter typically comprises several identical single phase H-bridge cells cascaded in series at its output side. This configuration is commonly referred to as a cascaded H-bridge (CHB), which can be classified as symmetrical if the dc bus voltages are equal in all the series power cells, or as asymmetrical if otherwise. The main disadvantage of the conventional cascaded H-bridge is that when the voltage level increases, the number of semiconductor switches increases and also the source required increases. In order to overcome this introduced a new topology of cascaded H-bridge. The main advantage of this topology is that the number of switches required is reduced and also the number of sources. Figure 1 shows the new cascaded five levels H-bridge multilevel inverter. It has additional one bidirectional switch connected between the first leg of the H-bridge and the capacitor midpoint, enabling five output voltage levels.

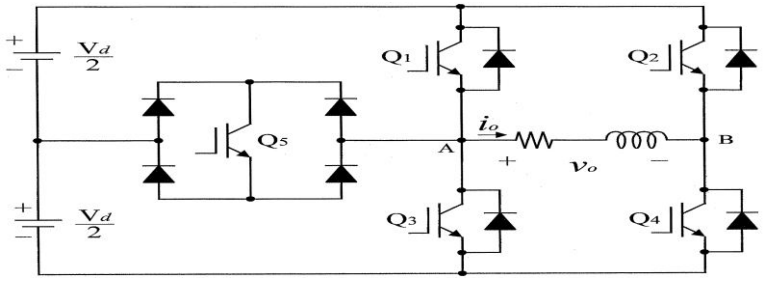

Fig. 1 Five level cascaded H-bridge multilevel inverter.

It has five output voltage levels i.e. V_{dc}, $V_{dc}/2$, 0, $-V_{dc}/2$, $-V_{dc}$. For getting the output voltage V_{dc}, the switches S_1S_4 need to be turned on. Similarly for output voltage $V_{dc}/2$ switches S_5S_4 need to be turned on, for 0 either S_3S_4 or S_1S_2 need to be turned on; for $-V_{dc}/2$ switches S_5S_2 need to be turned on; for $-V_{dc}$ switches S_3S_2 need to be turned on. The switch combinations are shown in table 1.

TABLE 1
FIVE- LEVEL CASCADED H-BRIDGE OUTPUT VOLTAGE

S1	S2	S3	S4	S5	V_{OUT}
ON	OFF	OFF	ON	OFF	V_{dc}
OFF	OFF	OFF	ON	ON	½ V_{dc}
OFF Or ON	OFF	ON Or OFF	OFF Or ON	OFF Or ON	0
OFF	ON	OFF	OFF	ON	$-1/2V_{dc}$
OFF	ON	ON	OFF	OFF	$-V_{dc}$

In the circuit shown in fig 1, single H-bridge module is capable of producing five level output voltage. Each inverter module is capable of producing 2E, E, 0, -E, -2E. That means by using two bridges 9 level output voltage is produced. The total output voltage is sum of the outputs of the inverter modules and the nine voltage levels are 4E, 3E, 2E, E, 0, -E, -2E, -3E, -4E. The advantages of this proposed circuit is number of switches are reduced. The cost and complexity is

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less in this circuit. To synthesize nine output voltage levels, it employs two independent dc voltage sources of 2*E* which are divided into two input sources *E* in order to secure an additional dc voltage source of *E*. The inverter module having a bidirectional switch produces 5-levels of output voltage (- 2*E*, -*E*, 0, *E*, 2*E*) by controlling of the switches. Since every output terminal of the inverter module is connected in series, the output voltage becomes the sum of the terminal voltages of each inverter. The circuit for nine level cascaded H-bridges is shown in figure 2, the gating signals for the inverter is generated by using multicarrier modulation.

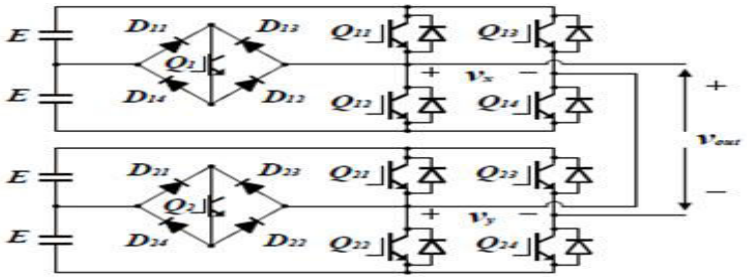

Fig.2. Nine level cascaded H-bridge multilevel inverter.

III.PWM MODULATION

In this inverter, the sinusoidal pulse width modulation is going to use. In the Sinusoidal pulse width modulation scheme, as the switch is turned on and off several times during each half-cycle, the width of the pulses is varied to change the output voltage. Lower order harmonics can be eliminated or reduced by selecting the type of modulation for the pulse widths and the number of pulses per half-cycle. Higher order harmonics may increase, but these are of concern because they can be eliminated easily by filters. The SPWM aims at generating a sinusoidal inverter output voltage without low-order harmonics. This is possible if the sampling frequency is high compared to the fundamental output frequency of the inverter.

The modulation index, *M* of the proposed multilevel inverter is defined by,

$$M = ½ (V_{ref} / V_{cr}) \quad (1)$$

Where Vref is the amplitude of the voltage reference and V_{cr} is the amplitude of the carrier signal. Multicarrier phase-shifted PWM (CPS-PWM) modulation is used to generate the PWM signals. The amplitude and frequency of all triangular carriers are the same as well as the phase shifts between adjacent carriers. Depending on the number of cells, the carrier phase shift for each cell, $\theta_{cr,n}$ can be obtained from,

$$\theta_{cr,n} = 2\pi(n-1)/N_c \text{ , } n= 1,2,\ldots\ldots\ldots N_c \quad (2)$$

For signal generation in each cell, two voltage references and one carrier signal are used. V_{ref} is defined by

$$V_{ref} = M \sin \omega t \quad (3)$$

$$V_{ref1} = | V_{ref} | \quad (4)$$

$$V_{ref2} = | V_{ref} - 1/2 | \quad (5)$$

Both references are identical but displaced by an offset equal to the carrier's amplitude which is ½. When the voltage reference is between 0<*vref*≤½, *vref1* is compared with the triangular carrier and alternately switches *S1* and *S3* while maintaining *S5* in the ON state to produce either ½*vdc* or 0. Whereas, when the reference is between ½<*vref*≤1, *vref2* is used and alternately switches *S1* and *S2* while maintaining *S5* in the ON state to produce either ½*vdc* or *vdc*. As for the reference between –½<*vref*≤0, *vref1* is used for comparison which alternately switches *S1* and *S2* while maintaining *S4* in the ON state to produce either –½*vdc* or 0. For a voltage reference between –1<*vref*≤–½, *vref2* is compared with the carrier to produce either –½*vdc* or –*vdc* alternately switches *S1* and *S3*, maintaining *S4* in the ON state. It is noted that two switches, *S4* and *S5*, only operate in each reference half cycle. This implies that both switches operate at the fundamental frequency while the others operate close to the carrier frequency. This allows the dc voltage to be switched at a low frequency so as to reduce the switching losses. Fig.3 shows the modulation scheme used for the proposed two-cell configuration and Fig. 4 shows a detail block diagram for generating the PWM signals.

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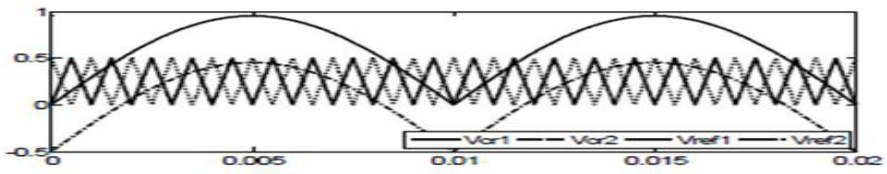

Fig 3. Multicarrier phase-shifted PWM for two-cell configuration.

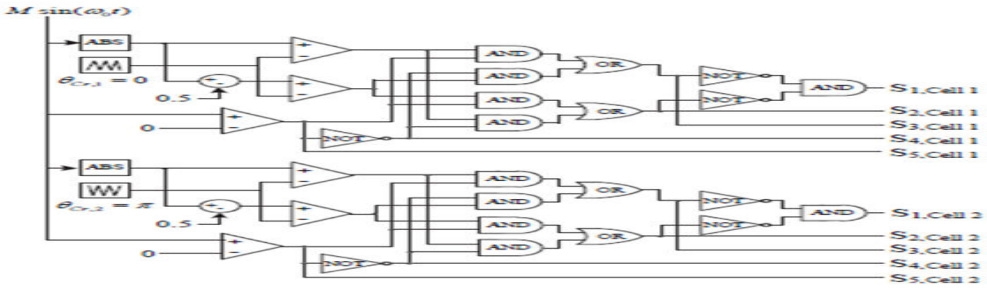

Fig 4. PWM signal generation with multicarrier phase-shifted modulation.

IV.SIMULATION RESULTS

The simulation model was designed using MATLAB/Simulink Software. The gating signals for the inverter are generated by using multicarrier pulse width modulation technique. The circuit was simulated with induction motor load. Figure 5 shows the circuit arrangement with multicarrier modulation.

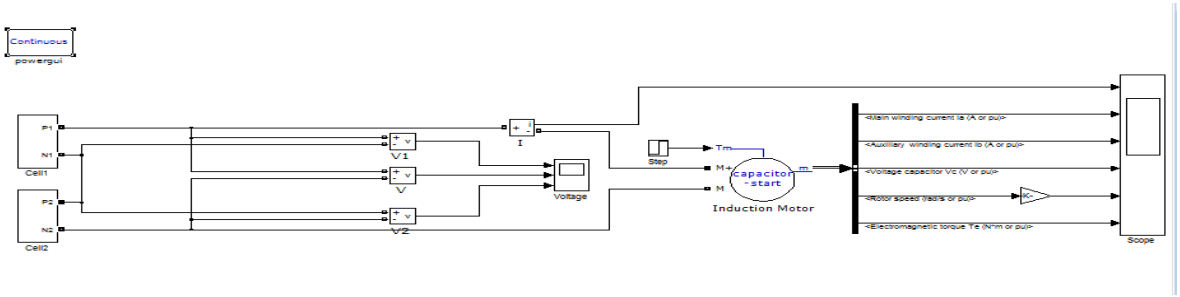

Fig 5. Circuit for Nine level Cascaded H-bidge Multilevel Inverter.

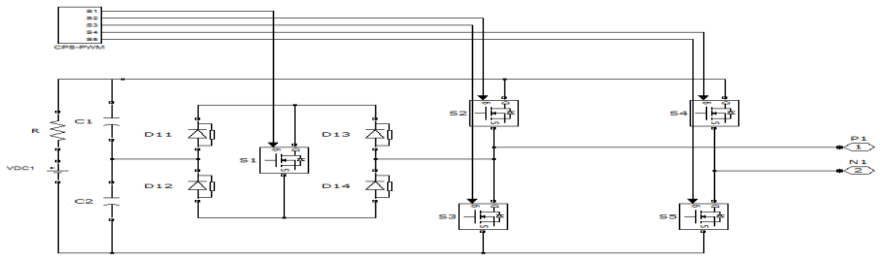

Fig 6. Circuit of cell 1.

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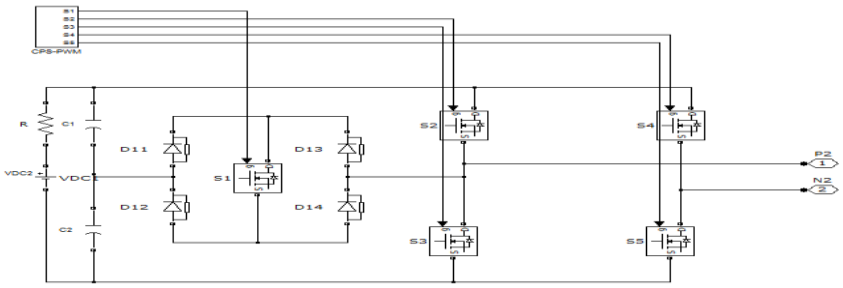

Fig 7. Circuit of cell 2

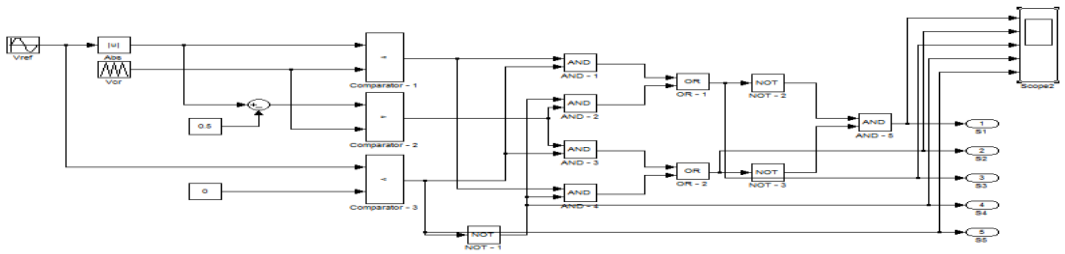

Fig 8. Circuit for PWM signal generation for cell 1.

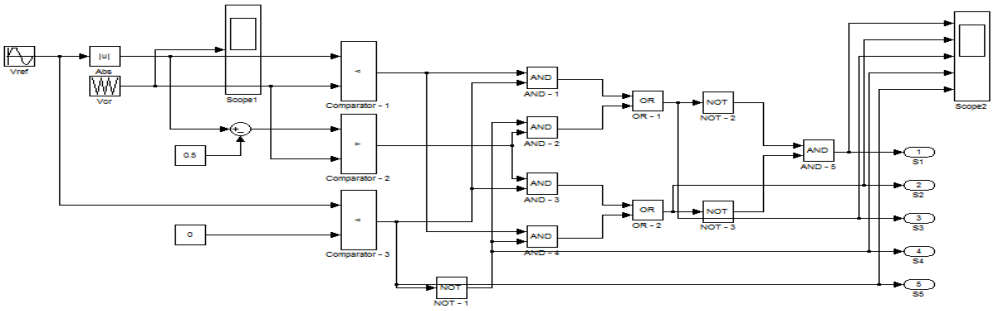

Fig 9. Circuit for PWM signal generation for cell 2.

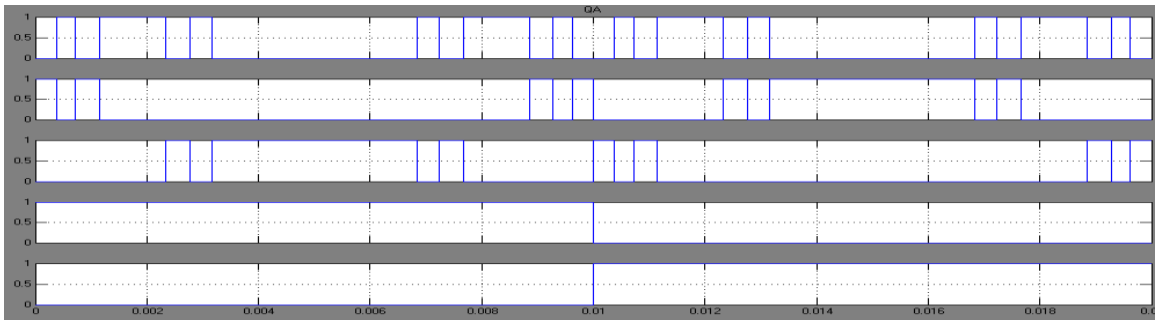

Fig 10. Switching pattern for cell 1.

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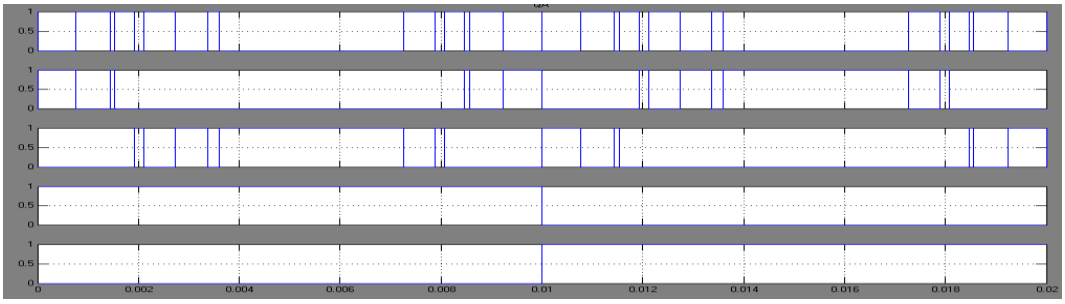

Fig 11. Switching pattern for cell 2.

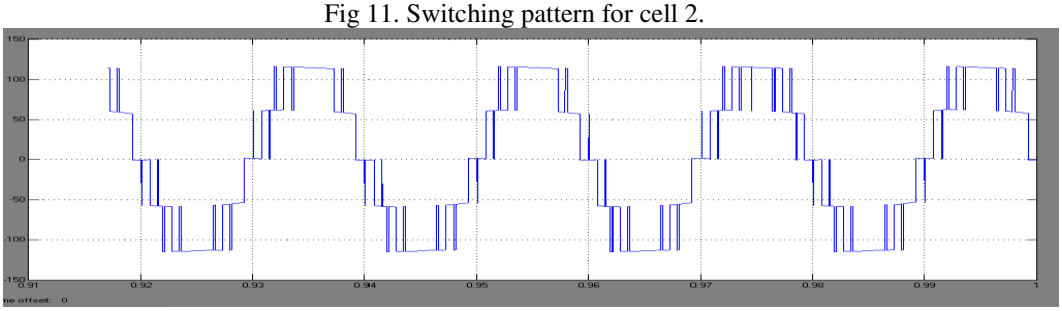

Fig 12. Five level output voltage waveform.

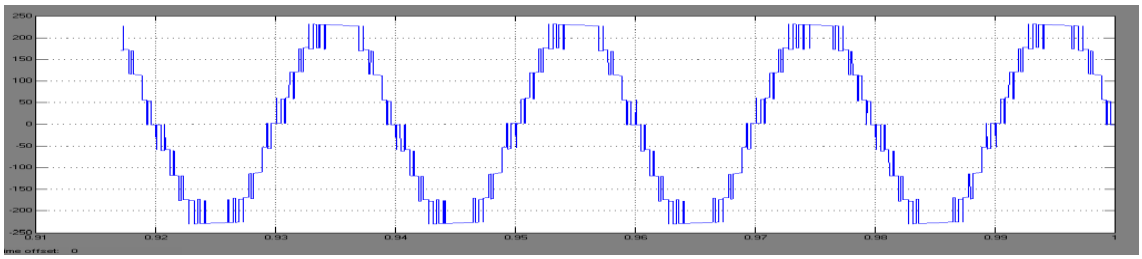

Fig 14. Output voltage waveform.

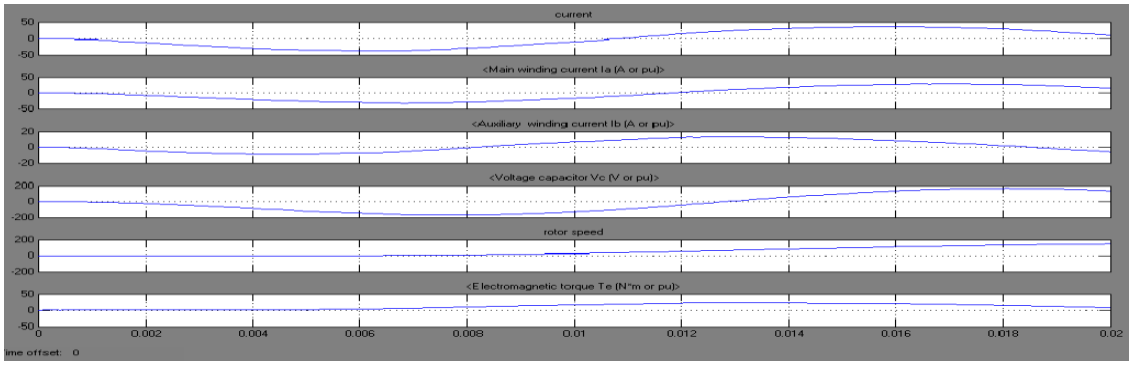

Fig 15. Output waveform.

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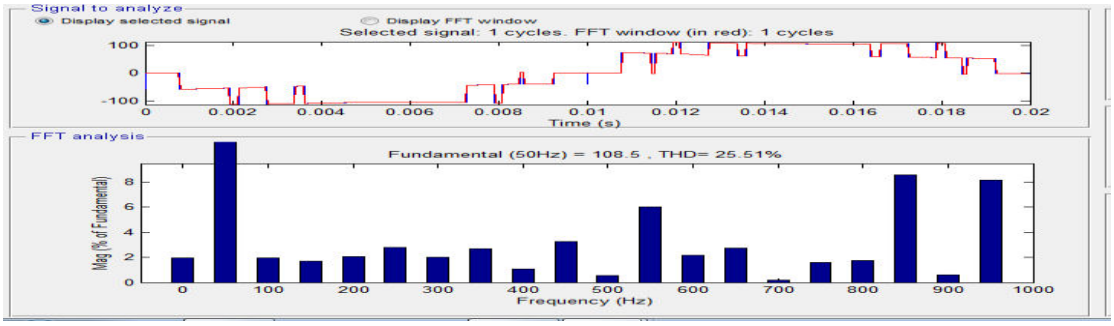

Figure 16. Five level cascaded H-bridge multilevel inverter with multicarrier modulation (cell 1), THD=25.51%.

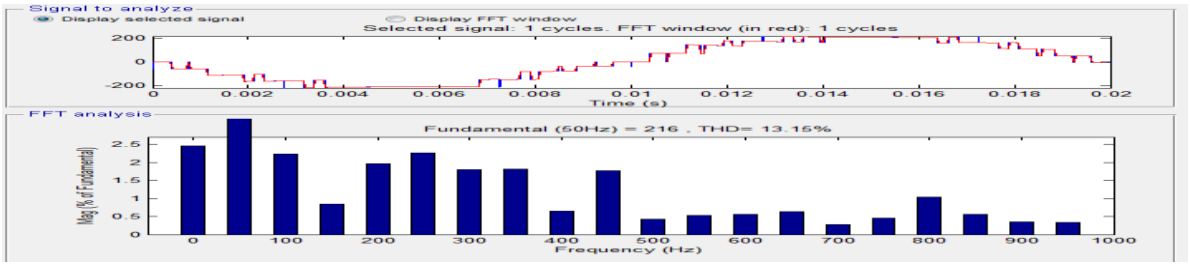

Figure 17. Nine level cascaded H-bridge multilevel inverter with multicarrier modulation, THD=13.15%.

Table 2 Simulation results

Multilevel inverter	THD (%)
Five level	25.51
Nine level	13.15

The simulation result shows that THD gets reduced significantly when the output voltage level increases.

V. HARDWARE IMPLEMENTATION

The circuit has hardware implemented with induction motor as load. An 8-bit microcontroller AT89S8253 was used to generate the PWM signals. The inverter was supplied by a 12V battery supply. The modulation index was set to M = 0.8. The specification of each cell is given in Table 3. Of the 10 MOSFETs, 2 form the bi-directional switches. There are 4 dc capacitors, 8 diodes and 6 full-bridge rectifiers.

Table 3
Specification parameters

Fundamental frequency f_o	50Hz
Carrier frequency f_c	2kHz
MOSFET	IRF540, 100V, 22A
Capacitor	2200µF, 200V
Diode	IN4007, 1000V, 30A

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The output voltage obtained is 32V and it is stepped up to 230V to drive the induction motor. The experimental setup is shown in figure 18.The output voltage waveforms are shown in figure 19 and 20.

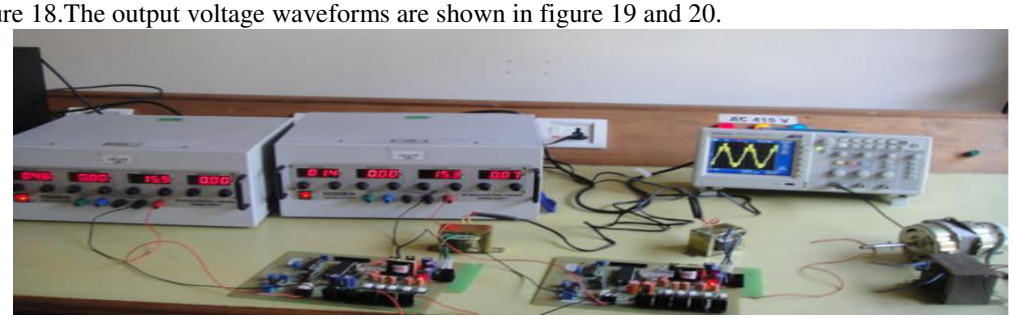

Fig 18. Experimental Setup.

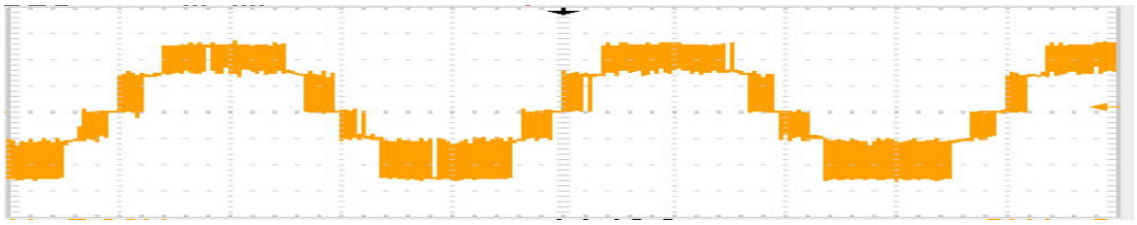

Fig 19. Five level output voltage waveform

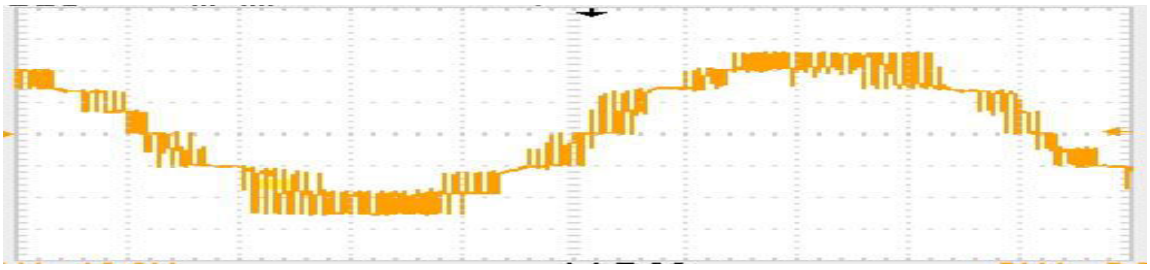

Fig 20. Nine level output voltage waveform

VI. CONCLUSION

Multilevel inverters have become an effective and practical solution for increasing power and reducing harmonics of ac waveforms. This project deals with the design and implementation of single-phase nine-level Cascaded H-bridge multilevel inverter for induction motor load with multicarrier phase-shifted PWM modulation method. The simulation and hardware implementation of 9-level cascaded H-bridge was made. Along with it, its harmonic analysis was done. The simulation results shows that the developed nine-level Cascaded H-bridge Multilevel inverter has many merits such as reduce number of switches, lower EMI, less harmonic distortion and the THD obtained is 13.15%. The study of this topology can also be extended to three phase induction motor and also to reduce the number of switches.

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