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NEW CASCADED H-BRIDGE MULTILEVEL INVERTER WITH IMPROVED EFFICIENCY

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Abstract: There are many limitations in extracting power from renewable energy resources. To minimize the power demand and scarcity we have to improve the power extracting methods. Multilevel inverter is used to extract power from solar cells. It synthesizes the desired ac output waveform from several dc sources. This paper focuses on improving the efficiency of the multilevel inverter and quality of output voltage waveform. Seven level reduced switches topology has been implemented with only seven switches. Fundamental Switching scheme and Selective Harmonics Elimination were implemented to reduce the Total Harmonics Distortion (THD) value. Selective Harmonics Elimination Stepped Waveform (SHESW) method is implemented to eliminate the lower order harmonics. Fundamental switching scheme is used to control the power electronics switches in the inverter. The proposed topology is suitable for any number of levels. The harmonic reduction is achieved by selecting appropriate switching angles. It shows hope to reduce initial cost and complexity hence it is apt for industrial applications. In this paper third and fifth level harmonics have been eliminated. Simulation work is done using the MATLAB software and experimental results have been presented to validate the theory.

Keywords: Multilevel Inverter, MATLAB, THD, Fundamental Switching Scheme and Selective Harmonics Elimination.

I. INTRODUCTION

Multilevel converters are mainly utilized to synthesis a desired single- or three-phase voltage waveform. The desired multi-staircase output voltage is obtained by combining several dc voltage sources. Solar cells, fuel cells, batteries and ultra-capacitors are the most common independent sources used[1]. One important application of multilevel converters is focused on medium and high-power conversion. Nowadays, there exist three commercial topologies of multilevel voltage-source inverters: neutral point clamped (NPC), cascaded H-bridge (CHB), and flying capacitors (FCs)[2]. Among these inverter topologies, cascaded multilevel inverter reaches the higher output voltage and power levels (13.8 kV, 30 MVA) and the higher reliability due to its modular topology[3].

Diode-clamped multilevel converters are used in conventional high-power ac motor drive applications like conveyors, pumps, fans, and mills. They are also utilized in oil, gas, metals, power, mining, water, marine, and chemical industries. They have also been reported to be used in a back-to-back configuration for regenerative applications[4]. Flying capacitor multilevel converters have been used in high-bandwidth high-switching frequency applications such as medium-voltage traction drives. Finally, cascaded H-bridge multilevel converters have been applied where high power and power quality are essential, for example, static synchronous compensators active filter and reactive power compensation applications, photovoltaic power conversion, uninterruptible power supplies, and magnetic resonance imaging. Furthermore, one of the growing applications for multilevel motor drives is electric and hybrid power trains.

For increasing voltage levels the number of switches also will increase in number. Hence the voltage stresses and switching losses will increase and the circuit will become complex. By using the proposed topology number of switches will reduce significantly and hence the efficiency will improve[5].

In high power applications, the harmonic content of the output waveforms has to be reduced as much as possible in order to avoid distortion in the grid and to reach the maximum energy efficiency[6]. The challenge associated with techniques is to obtain the analytical solutions of the non-linear transcendental equations that contain trigonometric

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terms which naturally exhibit multiple sets of solutions[7]. Generally the lower order harmonics are causing more effects when compared to the higher order harmonics. It is big challenge for any researcher to eliminate the third order harmonics using simple techniques, for a motor load its effects are high. This paper proposes method to eliminate lower order harmonics[8].

In this paper Selective Harmonics Elimination technique is used. Third and fifth order harmonics are eliminated by using this technique. The transcendental non-linear equations are solved using the numerical technique called Newton Raphson method. Cascaded H-bridge seven level inverter is modelled and harmonic analysis is carried out. Finally the hardware for the proposed topology is implemented and experimental results are presented.

II. H-BRIDGE MULTILEVEL INVERTER

The traditional two or three levels inverter does not completely eliminate the unwanted harmonics in the output waveform. Therefore, using the multilevel inverter as an alternative to traditional PWM inverters is investigated.

In this topology the number of phase voltage levels at the converter terminals is 2N+1, where N is the number of cells or dc link voltages. In this topology, each cell has separate dc link capacitor and the voltage across the capacitor might differ among the cells. So, each power circuit needs just one dc voltage source. The number of dc link capacitors is proportional to the number of phase voltage levels .Each H-bridge cell may have positive, negative or zero voltage. Final output voltage is the sum of all H-bridge cell voltages and is symmetric with respect to neutral point, so the number of voltage levels is odd.

Cascaded H-bridge multilevel inverters typically use IGBT switches. These switches have low block voltage and high switching frequency.

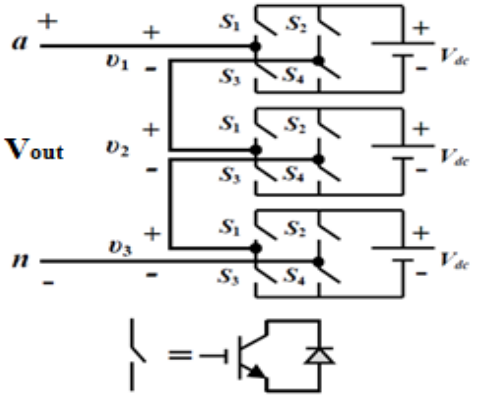

Fig 1. Cascaded H-bridge 7-level Inverter

Consider the seven level inverter; it requires 12 IGBT switches and three dc sources. The power circuit of inverter is shown in the figure 1. A cascaded H-bridges multilevel inverter is simply a series connection of multiple H-bridge inverters. Each H-bridge inverter has the same configuration as a typical single-phase full-bridge inverter.

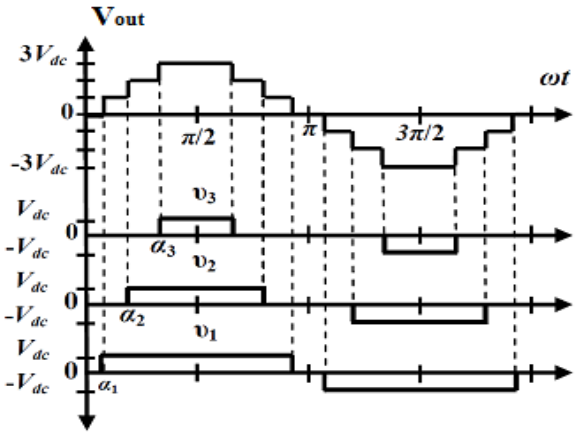

Fig 2. Output Voltage of cascaded H-bridge seven level inverter

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The cascaded H-bridges multilevel inverter introduces the idea of using Separate DC Sources (SDCSs) to produce an AC voltage waveform. Each H-bridge inverter is connected to its own DC source V_{dc}. By cascading the AC outputs of each H-bridge inverter, an AC voltage waveform is produced.

By closing the appropriate switches, each H-bridge inverter can produce three different voltages: $+V_{dc}$, 0 and $-V_{dc}$.

It is also possible to modularize circuit layout and packaging because each level has the same structure, and there are no extra clamping diodes or voltage balancing capacitors. The number of switches is reduced using the new topology.

This circuit is simulated using the MATLAB software. The results are shown in the later sections in detail.

III. PROPOSED TOPOLOGY

The main objective is to improve the quality output voltage of the multilevel inverter with reduced number of switches. An important issue in multilevel inverter design is that to generate nearly sinusoidal output voltage waveform and to eliminate lower order harmonics. A key concern in the fundamental switching scheme is to determine the switching angles in order to produce the voltage with fundamental frequency.

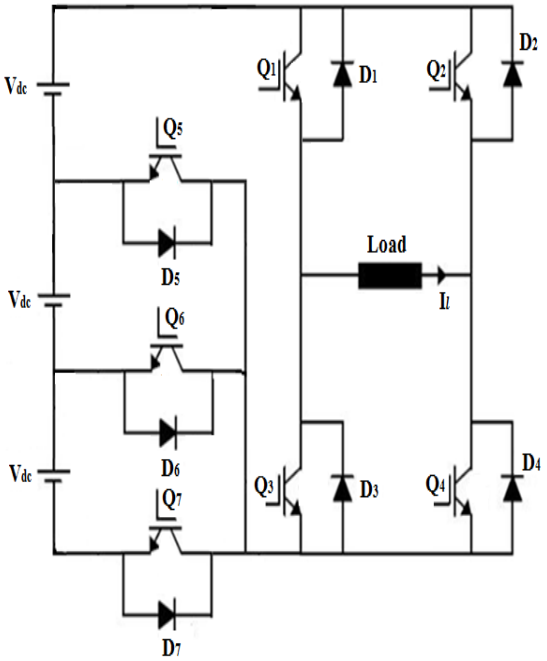

Fig 3 Proposed Power circuit for 7-level output

There are three modes of operation for the proposed 7-level multilevel inverter. These modes are explained as below.

Powering Mode: This occurs when both the load current and voltage have the same polarity. In the positive half cycle, when the output voltage is V_{dc}, the current pass comprises; the lower supply, D6, Q1, load, Q4, and back to the lower supply. When the output voltage is $2V_{dc}$, current pass is; the lower source, Q5, the upper source, Q1, load, Q4, and back to the lower source. When the output voltage is $3V_{dc}$, the current pass comprises: upper supply, Q1, load, Q4, Q7, lower supply. In the negative half cycle, Q1 and Q4 are replaced by Q2 and Q3 respectively.

Free-Wheeling Mode Free-wheeling modes exist when one of the main switches is turned-off while the load current needs to continue its pass due to load inductance. This is achieved with the help of the anti-parallel diodes of the switches, and the load circuit is disconnected from the source terminals. In this mode, the positive half cycle current pass comprises; Q1, load, and D2 or Q4, load, and D3, while in the negative half cycle the current pass includes Q3, load, and D4 or Q2, load, and D1.

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Regenerating Mode In this mode, part of the energy stored in the load inductance is returned back to the source. This happens during the intervals when the load current is negative during the positive half cycle and vice-versa, where the output voltage is zero. The positive current pass comprises; load, D2, Q6, the lower source, and D3, while the negative current pass comprises; load, D1, Q6, the lower source, and D4.

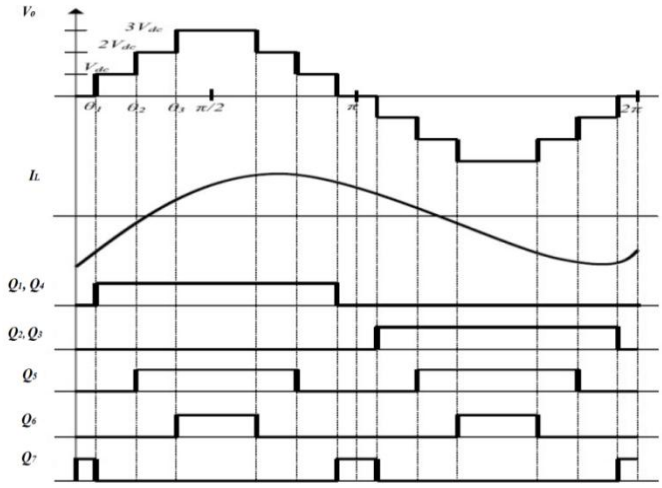

Fig 4 Waveforms of the proposed seven level inverter

From the figure 4 switching pattern for the various switches are explained. In this paper fundamental frequency switching scheme is employed which reduces the switching losses. Because the switching frequency is less in this method when compared to the other methods. Switching losses are directly proportional to the switching frequency.

IV. SELECTIVE HARMONICS ELIMINATION

The Selective Harmonic Elimination Stepped-Waveform (SHESW) technique is very suitable for a multilevel inverter circuit. Employing this technique along with the multilevel topology, the low Total Harmonic Distortion THD output waveform without any filter circuit is possible.

A. Fourier Series and Harmonics Elimination Theory

After applying Fourier theory to the output voltage waveform of multilevel converters, which is odd quarter-wave symmetric, we can find the Fourier expression of the multilevel output voltage as (1). If the DC voltages are equal in the multilevel converter, the equation for the fundamental frequency switching control method can be expressed as:

$$V(t) = \sum_{n=1,3,5....}^{\infty} \frac{4V_{dc}}{n\pi} (\cos(n\theta_1)\,(\cos(n\theta_2) + (\cos(n\theta_3) + \ldots + (\cos(n\theta_s))\sin(n\omega t) \quad (1)$$

From the equation, it can be seen that the output voltage has no even harmonics because the output voltage waveform is odd quarter-wave symmetric. It also can be seen from (2) that the peak values of these odd harmonics are expressed in terms of the switching angles θ_1 ,θ_2, … and θs. Furthermore, the harmonic equations produced from (2) are transcendental equations.

Based on the harmonic elimination theory, if one wants to eliminate the n_{th} harmonic, then

$$\cos(n\theta_1) + \cos(n\theta_2) + .. + \cos(n\theta_s) = 0 \quad (2)$$

That means to choose a series of switching angles to let the value of the nth harmonic be zero. Therefore, an equation with *s* switching angles will be used to control the s different harmonic values. Generally, an equation with s switching angles is used to determine the fundamental frequency value, and to eliminate s-1 low order harmonics.

For an equation with three switching angles, (2) becomes

$$V(t) = \sum_{n=1,3,5....}^{\infty} \frac{4V_{dc}}{n\pi} (\cos(n\theta_1) + (\cos(n\theta_2) + (\cos(n\theta_3))\sin(n\omega t) \quad (3)$$

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B. Transcendental Equations to Solve

In this paper we derived harmonic equations for eliminating the 3rd and 5th order harmonics. The resulting harmonic equations are:

$$\cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) = \frac{\pi V_1}{4V_{dc}} \quad (4)$$

$$\cos(3\theta_1) + \cos(3\theta_2) + \cos(3\theta_3) = 0 \quad (5)$$

$$\cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3) = 0 \quad (6)$$

To simplify the expression, (4) can be written as

$$\cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) = m \quad (7)$$

Where

$$m = \frac{\pi V_1}{4V_{dc}} \quad (8)$$

These harmonic equations (4)-(6) are transcendental equations. They are difficult to solve without using some sort of numerical iterative technique. Here Newton Raphson method is employed for solving these equations.

C. Solving the Harmonic Equations using Newton Raphson Method

To solve the harmonic equations by resultant theory, they must be changed into polynomials. First, change the variables,

$$x_1 = \cos(\theta_1) \quad (9)$$

$$x_2 = \cos(\theta_2) \quad (10)$$

and

$$x_3 = \cos(\theta_3) \quad (11)$$

Also, use the following trigonometric identities:

$$\cos(3\theta) = 4\cos^3(\theta) - 3\cos(\theta) \quad (12)$$

$$\cos(5\theta) = 5\cos(\theta) - 20\cos^3(\theta) + 16\cos^5(\theta) \quad (13)$$

Then, apply them to the transcendental harmonic equations above, and the following polynomial harmonic equations can be found.

For the fundamental frequency harmonic:

$$P_1(x_1, x_2, x_3) = \sum_{n=1}^{3} x_n - m = 0 \quad (14)$$

For the 3rd harmonic:

$$P_1(x_1, x_2, x_3) = \sum_{n=1}^{3} (4x_n^3 - 3x_n) = 0 \quad (15)$$

For the 5th harmonic:

$$P_1(x_1, x_2, x_3) = \sum_{n=1}^{3} (5x_n - 20x_n^3 + 20x_n^5) = 0 \quad (16)$$

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The polynomial equations can be solved by using the Newton Raphson method. The following are steps for solving the equations. Substitute the initial guesses for variables. Then form the jacobian matrix with newton's formula. Repeat the same steps until the solutions to converge. Thus the solutions obtained are given below

$$\theta_1 = 8.76655°$$
$$\theta_2 = 28.6886°$$
$$\theta_3 = 54.9395°$$

V. EXPERIMENTAL RESULTS AND DISCUSSION

To validate the proposed topology and theory, hardware of the 7 level cascaded H-bridge multilevel inverter has been built using the MOSFET as the switching devices.

DC source voltage is getting by using diode rectifier circuit which is placed infront of the inverter circuit. Three equal DC source voltages are applied which is equal to 75 volts. Hence finally the output AC voltage for each phase is equal to 225 volts. The MOSFET driver ICs are employed to drive the MOSFET switches.

The MOSFETs are switched ON and OFF by using the PWM pulses which are generated by using the microprocessor called Renasas. Controller algorithm for the switching is written in the high level language and then it is embedded in the Renasas microprocessor. The output terminal of the inverter is connected to three phase squirrel cage induction motor. The experimental results are exposed in the figures 6 and 7. The output of the seven level inverter is 400 volts with frequency of 50Hz.

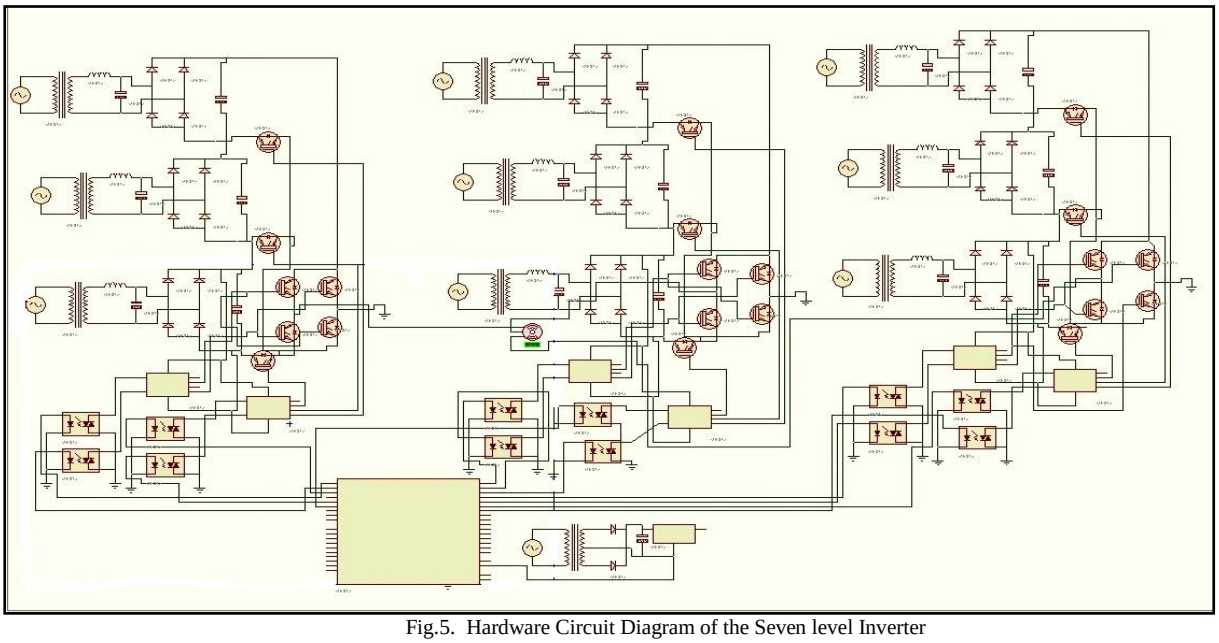

Fig.5. Hardware Circuit Diagram of the Seven level Inverter

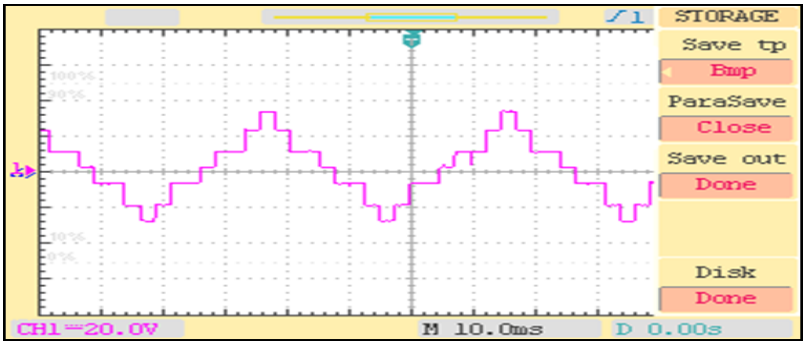

Fig 6. Seven level output voltage waveform for R phase

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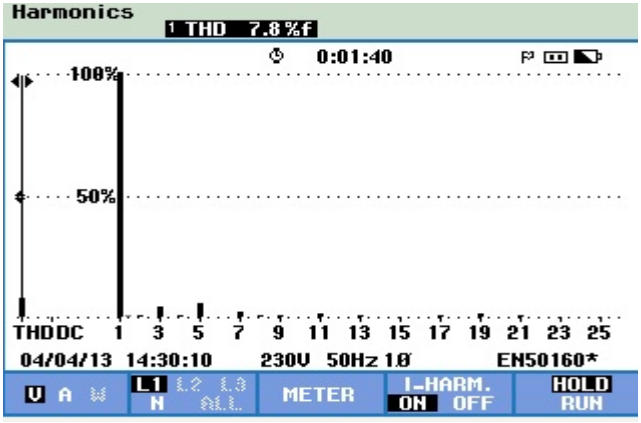

Fig 7. Power quality analyser output

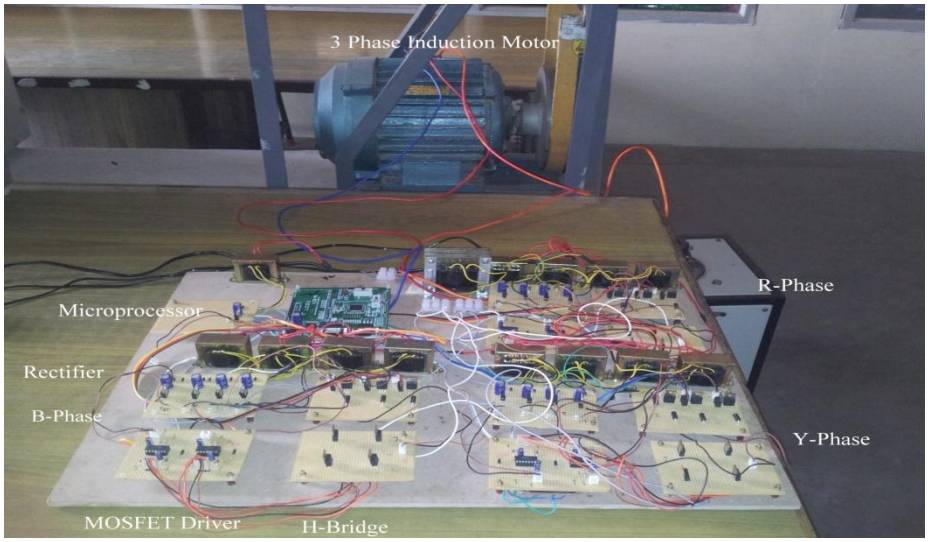

Fig. 8 Hardware Setup

By using the power quality analyser equipment the THD value for the output voltage of the inverter is measured. The measured values and the simulation results are coordinates with each other. The value of THD is found to be 7.8%. The experiment results are showing that this topology is well suited are the industrial applications.

VI. CONCLUSION

The proposed new cascaded H-bridge multilevel inverter fed induction motor using equal DC sources was developed and validated with the hardware. The fundamental switching scheme is employed using the microprocessor. By using the Selective harmonics elimination the firing angles are calculated and fed to the inverter for its operation. Finally using the power quality analyser the harmonics are measured and shown. In the conventional H- bridge multilevel inverter for seven level output 12 switches are needed whereas in new topology it is only 7. The percentage of reduced number of switches is explained with the help of the table 1 showm below.

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Table 1: Percentage of Reduction in Switches

Inverter Type		7-level
Number of Switches used	Cascaded H-Bridge	12
	Proposed Topology	7
% of switch reduction		41.667

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BIOGRAPHY

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