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ON AUTOMATIC ADJUSTMENT OF All BJTs OF A CURRENT MIRROR IN CONSTANT CURRENT REGION

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ABSTRACT: The impact of tiny chip has been far-reaching. Many of the electronic products of today, could not have been developed without it. Platform for these chips has been provided by Integrated Circuits (ICs). Since 40 decades ICs have been far revolutionized. Various advancement have been made in these ICs; but still there are some conditions imposed by the designers for proper working of IC. One of such condition exist in biasing of IC. While designing the IC from Bipolar Junction Transistor (BJT), designers introduce that the collector voltage of output BJT used in biased circuit should be greater than a defined minimum value. It implies that user should check every time that whether the circuit is following the specified condition or not. The proposed biasing circuit design in this paper has no such condition and the user will get much freedom.

Keywords: Current Mirror, Active Mode, Beta (β), Early Effect, Scale Current.

I. INTRODUCTION

Since 1971 Integrated Circuits are the essence of Electronics Engineering. Transistors are frequently used active device in these ICs. For operation of ICs proper biasing is essential. Nowadays several 'active biasing' techniques have been used to bias an IC (e.g. Simple Current Mirror, Current Mirror with Better β Insensitivity, Cascode Current Mirror, Wilson Current Mirror, Widlar Current Source). Since last 20 decades improvements have been carried out in biasing techniques. Laura Sanchez-Gonzalez, Gladys Ducodray-Acevedo presented a novel approach to improve the previous current mirrors and increased the current input range with a lower error percentage and a high accuracy low voltage dynamic self-biasing ([6]). Adjustable gain linear current gain mirrors are also presented. According to A. K. Gupta, J. W. Haslett and F. N. Trofimenkoff, it can produce linear gain over several decades of signal current ([5]). Low voltage application current source has been designed. The use of low voltage application current source improved the common mode input range and the common mode rejection ratio of fully-balanced single ended differential amplifier by Fan You, S.H.K. Embabi, J.F. Duque- Carrillo and Edgar Sanchez- Sinencio ([7]). But all of these biasing techniques impose a condition on the output BJT, regarding its collector voltage i.e. output transistor should be operated in such a manner that its collector voltage must be higher than a certain value. And during our operation we must keep this value in mind. In the following section you will get familiar with a design that can bias an IC without imposing any condition on the collector voltage of output transistor. The bias circuit is such that it will set its output transistor in the require mode (active mode).

II. CIRCUIT DESCRIPTION & SPECIFICATIONS

Schematic of bias circuit is such that the base of transistor Q_1 (npn) and Q_2 (npn) are tied together as in Fig. 1. Their emitter terminals are shorted with ground. Thus Q_1 and Q_2 are forming mirror. Q_3 (npn) is introduced to reduce the dependency of β on output current. Q_4 (pnp) is to adjust Q_3 in active mode. Base of Q_4 is grounded and its emitter has two branches, one going towards base of Q_3 with resistance R_2 and the other one towards collector of Q_2 with resistance

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R_3. Current flowing in all the branches are shown in Fig. 1. R_1 is to generate desired reference current in whole circuit with the help of supply voltage.

$R_1 = 3\ k\Omega$

$R_2 = 1\ k\Omega$

$R_3 = 1\ k\Omega$

$R_4 = 0.002\ k\Omega$ (load resistance; adjustable according to our need)

Source voltage = 15 Volts

III. CIRCUIT ANALYSIS

In Fig. 1 voltage at collector of Q_1 is $V_{C1,}$

$V_{C1} = V_{BE3} + V_{BE1}$ ———— (1)

V_{BE3} = Voltage across base emitter junction of Q3

V_{BE1} = Voltage across base emitter junction of Q_1

"For ON transistor V_{BE} should lies between 0.6 to 0.7 Volt" because input characteristic of bipolar junction transistor is like diode in forward bias condition. Hence if Q_1 and Q_3 is On,

V_{C1} or $V_{CE\ 1} = 1.4$ Volt

Taking $V_{BE3} = V_{BE1} = 0.7$ Volt

Therefor Q_1 is in active region automatically because,

$V_{CE} \geq 0.2$ Volt for BJT to be in Active Mode (i.e. in Constant Current mode)

Now,

$V_{BE1} = V_{BE2}$

Since, $I_C = I_S \exp(V_{BE}/V_T)$ —— collector current without early effect.

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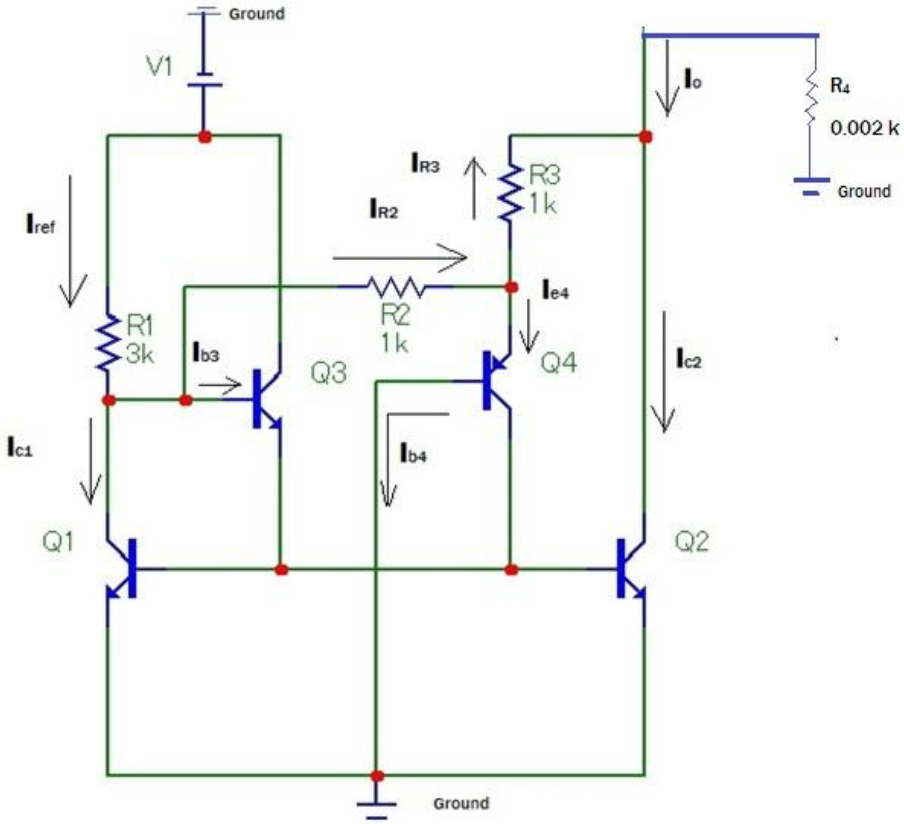

Fig. 1 Proposed circuit design for improvement in Current Mirror circuit

V_T is thermal voltage having value 0.026 Volts at 300 K temperature.

$V_T \ln (I_{C1} / I_{S1}) = V_T \ln (I_{C2} / I_{S2})$ ———— (2)

I_{C1} = Collector current of Q_1

I_{C2} = Collector current of Q_2

I_{S1} = Scale current of Q_1

I_{S2} = Scale current of Q_2

Since Q_1 and Q_2 are matched hence,

$I_{S1} = I_{S2}$

Therefore (2) becomes

$I_{C1} = I_{C2}$

Q_3 transistor is employed for better β insensitivity i.e. if effect of β is taken into account, then Q_3 will act such that it will divide very less current [$I_{B3} = 2I_{C1} / \{\beta(\beta+1)\}$; for more information refer Reference [1]] from I_{REF} and hence,

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$I_{REF} \approx I_{C1}$

Now the main action is employment of Q_4 (pnp BJT) in this circuit.

For this transistor to act as a perfect constant current bias circuit Q_2 should be in active region (i.e. constant current region).

"Typical value of V_{CE} varies from 0.1 to 0.3 Volts for transistor to be in active region".

In Fig. 1 for time being let us suppose that $R_2 = 0\ \Omega$ then

V_{EB} of $Q_4 > 0.7$ Volts i.e. Q_4 is ON

R_3 ($\approx k\Omega$) is introduced, so that negligible current go through R_3 and hence,

$I_o \approx I_{C2}$

And $V_{EC4} = V_{C1} - V_{BE1} \approx 1.4 - 0.7 \approx 0.7$ Volts

V_{EC4} = drop across emitter-collector junction of Q_4

Therefore V_{CB2} = drop across $R_3 + V_{EC4}$

V_{CB2} = drop across collector base junction of Q_2

And $V_{CE2} = V_{BE2} - V_{BC2}$

V_{CE2} = Voltage across collector-emitter junction of Q_2

V_{BE2} = Voltage across base emitter junction of Q_2

$V_{CE2} = 0.7 - \{-(V_{CB2})\}$ ———— (3)

$V_{CE2} = 0.7 - \{-(\text{drop across } R_3 + V_{EC4})\}$

Since,

(Drop across $R_3 + V_{EC4}$) > 0.7 Volts

Therefore (3) becomes,

$V_{CE2} > 1.4$ Volts

Hence Q_2 is in active region, and there is no need to take care of output transistor collector voltage value for proper biasing.

Now R_2 is employed as a current limiting resistor, so that less current will draw from R_1 because in absence of R_1 emitter of Q_4 will draw more current. Therefore

$I_{C1} \approx I_{REF}$

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And mostly all current which is flowing in R_2 go towards emitter of Q_4 because of R_3 (i.e. R_3 will draw less current). Since Q_4 is a pnp transistor hence it will also draw less current from R_1 but not as much less as current flowing in R_3. Hence overall effect is that very less current will go towards R_2 and that current is mostly divided at emitter of Q_4.

IV. COMPARISON FROM NORMAL CURRENT MIRROR WITH BETTER BETA INSENSITIVITY

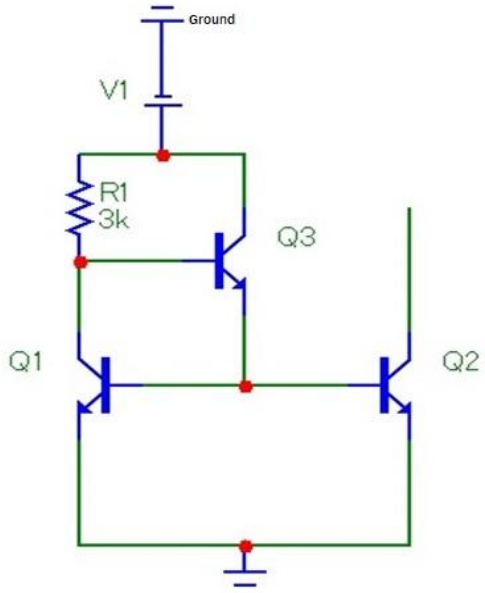

Fig. 2 Normal Current Mirror with Better β Insensitivity

In Fig.2, to act it as a perfect constant source V_{CE} of Q_2 should be greater than 0.2 Volts i.e. must be adjusted such that at every level of analysis we must take care of this V_{CE} value.

But in Fig.1 there is no need to take care V_{CE} value of Q_2 (or output transistor) because it automatically adjust itself in active region (i.e. a perfect constant current source).

V. EXPERIMENTAL RESULTS

When 15 Volts DC source is employed and R_1, R_2, R_3 are taken as mentioned earlier.

$V_{BE1} = V_{BE2} = 0.68$ Volts (Q_1 and Q_2 are ON)

$V_{BE3} = 1.38 – 0.68 = 0.7$ Volts (Q_3 is ON)

$V_{CE1} = 1.38$ Volts (Q_1 is in active mode)

$V_{CE2} = 1.1$ Volts (Q_2 is in active mode)

$I_{R3} = 0.6$ mA (very low)

$I_{REF} = 5.1$ mA

$I_O = 5.0$ mA

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I_{R3} = Current flowing in R_3 resistor

VI. CONCLUSION

Though there are several Integrated Active Biasing circuits and also some of them have remarkable level of stability of output current; but all active biased circuits suffer from a required value of collector voltage of its output transistor. This illustrated design simplifies this flaw. Hence by using this design we can bias our IC chip more efficiently without requiring adjustment of voltage at collector terminal. We will be more flexible in BiCMOS process using this design.

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BIOGRAPHY

Kimmi Verma, She is professor of Instrumentation & Control Engineering, in Galgotias College of Engineering & Technology, Greater Noida, India. She is a member of IEEE, IETE society. Presently, she is pursuing PhD from Banasthali Vidyapith. Her M.Tech degree is in Microelectronics from G.B.Technical University. She has published a book on "Analog and Digital Electronics" with University Science Press. She has authored several research papers in the field of Image Processing, Analog Circuit Designing in various journals and conferences.

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