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Performance Enhancement of UPQC Using Multi-Loop Control Scheme

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Abstract—Power quality has become an important issue nowadays for several reasons, e.g. modern society's growing dependence on electricity and the fact that poor power quality may generate significant economic losses in few moments. Probable power quality problems are, e.g. harmonics, flicker, voltage dips and supply interruptions. The power quality may be improved by using filters and compensators. Custom Power (CP) devices that mitigate these power quality problems have gained more attention in the recent decades. Unified Power Quality Conditioner (UPQC) is one of the CP devices whichmitigates both load current and supply voltage problems simultaneously. In this paper the development of UPQC with transformer less cross phase connected UPQC has been implemented. The control strategy incorporated is much similar to Dynamic Voltage Restorer (DVR).This scheme was found beneficial and the simulation (using MATLAB/SIMULINK) results prove that the voltage and current control was found good and the harmonics in the system were also reduced.

IndexTerms—Power quality, Harmonics, UPQC, Voltage Source Converter (VSC)

I. INTRODUCTION

Power quality phenomena include all situations in which the supply voltage (voltage quality) or load current (current quality) waveforms deviate from the sinusoidal waveform at rated frequency with amplitude corresponding to peak value for all the phases for any three-phase system. In recent years, the term Power Quality (PQ) has gained significant importance, especially in electrical distribution side. As per international standards, the term power quality can be defined as the physical characteristics of the electrical supply provided under normal operating conditions that do not disrupt or disturb the user's processes. The disturbances in voltage (harmonics, sags, swells) may cause the tripping of sensitive electronic equipment which can lead to disastrous consequences in industrial plants, such as,unexpected results or a termination of the whole production line. These events are common in industrial sectors and cause high economical damage. In the above scenario, it is the source that disturbs the load/ sensitive equipment. To avoid heavy economical losses, the industrial customers often install mitigation devices/ equipment's to protect their own plants from such kind of disturbances.The growing use of power electronics based equipment's in modem plants is resulting in a load which is sensitive and harmonics producing in nature. Interestingly, this equipment's generally produce distortion in currents and/or voltages. Thus, there is a new trend to install mitigating equipment's that can serve the dual purpose, to both the utility as well as to the customer. Thus with the implementation of Custom Power Devices in the distribution side, Power Quality is enhanced. One of the most effective solutions to power quality issues in the distribution side is the installation of Unified Power Quality Conditioner (UPQC). UPQC is supported for alleviating all the voltage and current related problems (imbalances, Harmonics etc). Conventional UPQC [1] is constituted of two Voltage Source converters (VSC), an injection transformer and a common dc link as shown in Fig. l(a). The presence of injection transformer can create problems like offset due to energisation of transformers, increased losses in transformer windings and high cost of the system. Thus there is a need for a better injecting device. A DC isolation circuit was proposed in [4]. This implementation increases the complexity of the system along with the increase in the cost of the system. Thus, here in this paper, injection transformer as well as the DC isolation circuit is replaced with a series capacitor which acts as 'Voltage Injecting' source to the line. With the use of a series capacitor as injecting device [5], the cost and the complexity of the system is reduced and the system was found more efficient.

The conventional UPQC can eliminate three phase faults alone. The system remains idle forsingle phase faults. The cross phase connected UPQC enables to

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overcome the problems related to single line faults [6]. The cross phase connection enables injection of voltage to a faulty phase from a healthy phase. The cross connection in phase is given at the load side as shown in Fig. l(b). Unlike conventional UPQC, here each phase is implemented with half bridge configuration VSCs and separate DC links for each phase. This configuration provides better control of each phase keeping the cost also minimal.

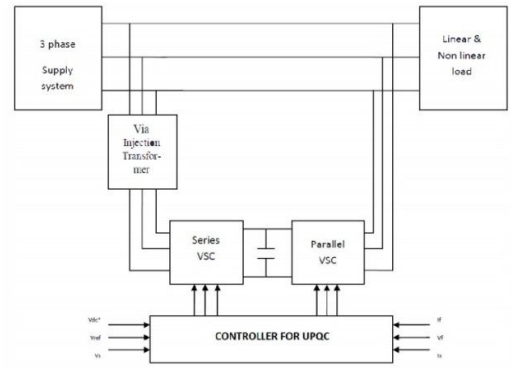

Fig 1 (a) - Conventional UPQC

Control scheme of the proposed UPQC is also consideredhere in this paper. Various control strategies have beenproposed for UPQC. Some of them are PQ theory [7], wavelettransform [9], neural networks [10], fuzzy algorithm [11], Fourier transform theory [8], State feedback control law [2],power angle control (PAC) concept [13].

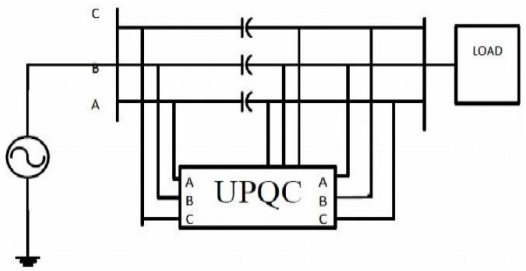

Fig 1 (b) - Single line diagram for the proposed system with crossconnected phaseat load side

In this paper, the control strategy implemented is muchsimilar to DVRs. The control strategy of a transformer-lessDVR is discussed in [5]. The control is implemented basedupon the series capacitor voltage and the inductor currentfeedbacks. The design of the series capacitor and the inductorsare obtained from [15].

II. SYSTEM DESIGN

A. Basic System Design

The basic circuit diagram of the proposed system is shownin Fig. 2. The series and shunt VSC is not the conventional fullbridge configuration. There are three UPQC modulescorresponding to each phase. Each module consists of twoVSCs in half bridges configuration and a split capacitor DClink. Out of the two halfbridges, one acts as the series VSCand other as Parallel VSC. The system is more efficientbecause of different DC link voltages corresponding todifferent phases. Whenever a fault occurs, the system restores immediately and more efficiently. The UPQC module for phaseA is shown in Fig 3. Unlike the conventional UPQC, here theability to eliminate faults occurring due to the single phasing isobtained. Cross phase connection enables the system toeliminate this fault. The elimination of single phase fault can be explained very well. The shunt VSC of the Phase C is connected to Phase A of the load terminal, when Phase C has asingle phase fault occurred. The current in Phase A is absorbedby the shunt VSC and the series VSC for phase C works. This enables injecting series voltage via the capacitor. Themagnitude and phase of the injected voltage in this case will besame as Phase C since the module corresponding to phase Cworks here. This advantage of the proposed system can widely used.

B. Controller for Series VSC

The main aim of the series VSC is to compensate for voltage imbalances. For any system, when there are imbalances, the voltage can be resolved into three components. The positive sequence will be always in phase with the supply system. The voltage equation with resolved components is as follows:

$$\begin{bmatrix} V_{sa} \\ V_{sb} \\ V_{sc} \end{bmatrix} = V_{sp} \begin{bmatrix} \cos(\omega t + \theta_p) \\ \cos(\omega t - \frac{2\pi}{3} + \theta_p) \\ \cos(\omega t + \frac{2\pi}{3} + \theta_p) \end{bmatrix} + V_{sn} \begin{bmatrix} \cos(\omega t + \theta_n) \\ \cos(\omega t + \frac{2\pi}{3} + \theta_n) \\ \cos(\omega t - \frac{2\pi}{3} + \theta_n) \end{bmatrix} \quad (1)$$

Here V_{sp} and $V_{sn}$are the magnitude of the positive and negative components respectively. $\theta_p$and θ_n are the phases angles of positive sequence component and negative sequence component respectively.

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The ωt andθ_p are extracted using the SPLL (software phase locked loop). The control signals for the series is provided as depicted in Fig 3.The design for the system is based on the control system analysis.

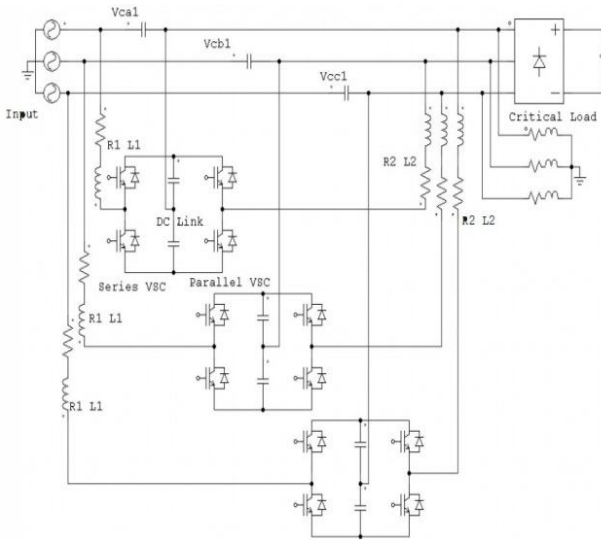

Fig 2 - circuit diagram for the proposed strategy

From the flowchart, we obtain control block diagram as shown in Fig. 4. The various parameters of the system are obtained by obtaining the overall closed loop transfer function and then performing stability analysis on the system. Based on the stability analysis results and selecting a desired damping ratio, the parameters are calculated.

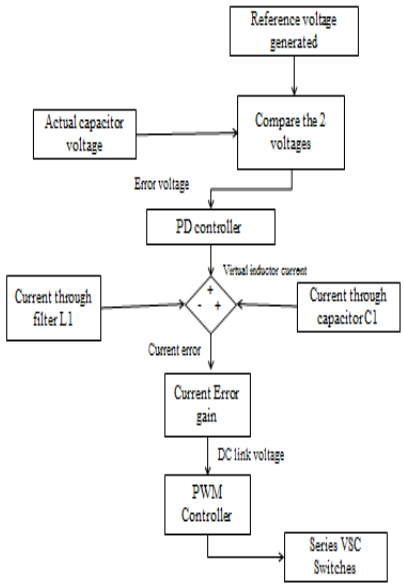

Fig 3 Flowchart for the Series VSC controller

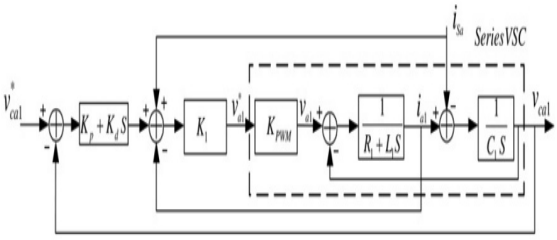

Fig 4 - Control Block diagram - Series VSC

Here PWM controller is modeled as a unity gain system (Kpwm = 1). From the total transfer function of the system, V_{ca1}, which is the actual capacitor voltage, is obtained as in the equation below:

$$V_{ca1} = G_1 V^*_{ca1} + G_2 i_{sa} \quad (2)$$

Where, G_1 and $G_2$are transfer function with input V^*_{ca1}(Capacitor Voltage calculated) and i_{sa} (Source current) respectively. Thus transfer function G_1 and G_2will consist of all the parameters K_1 (Current Error gain), K_p (Proportional Gain of PD controller) and K_d (Derivative gain of PD controller)

From calculation, the values were found to beK_1= 25, K_p=26 &K_d = 0.005. Thus the control system for series

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VSC was analyzed and the switching frequency of the IGBT switches of series UPQC used was 5 KHz.

C. Controller For Parallel VSC

The major concern for the parallel VSC is to compensate for unbalances and reactive power components of the load currents and reduce the harmonics in the current. Here a reference current is generated based on the power balance theory and instantaneous power theory. By applying power balance relationship & the theory of instantaneous active power and reactive power we obtain the reference current in a-ß reference frame. Here PLOSS is calculated as the power loss in the resistors through which UPQC module is connected to the lines.The reference current generation in abc reference frame is depicted in Fig 4

Thus the reference current generated in a-ß reference frame is transformed using C_{PQ}^{-1}matrix which is as given below:

$$\begin{bmatrix} i_{\alpha f}^{*} \\ i_{\beta f}^{*} \end{bmatrix} = C_{PQ}^{-1} \begin{bmatrix} P_s \\ q_s \end{bmatrix} = \begin{bmatrix} V_\alpha & V_\beta \\ V_\beta & V_{-\alpha} \end{bmatrix} \begin{bmatrix} P_s \\ q_s \end{bmatrix} \quad (3)$$

Where, the voltages V_α, $V_\beta$are given as below

$$V_\alpha = V_{sd} * \cos((\omega t)+\theta_p)$$

$$V_\beta = V_{sd} * \sin((\omega t)+\theta_p)$$

$V_{sd}$is the positive sequence component of supply. The reference current generated in a-ß reference frame is converted to abc reference frame. And we obtain currenti_{sa}^{*}, $i_{sb}^{*}$and i_{sc}^{*} for phases A, B and C phases respectively.

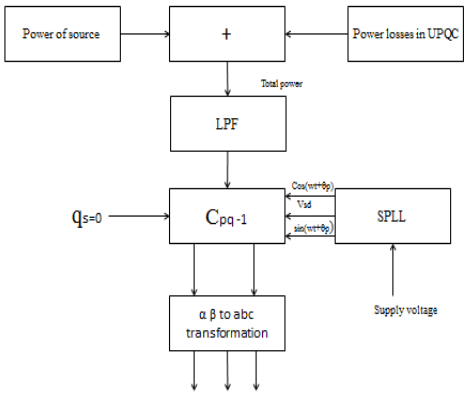

Fig 4 - Reference current generation

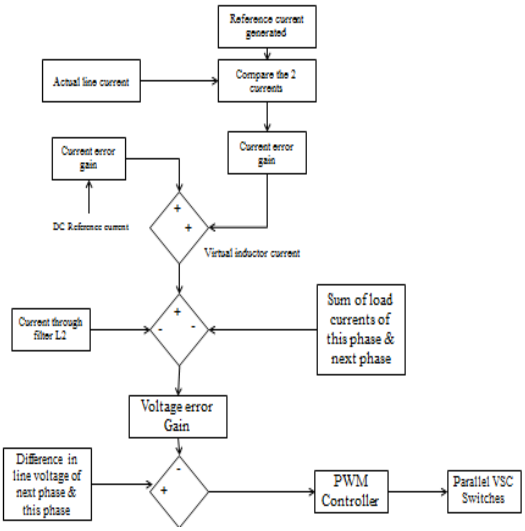

Fig 5 Flow chart for parallel VSC

The flowchart for the parallel VSC control is shown in Fig 5. The DC link reference voltage is calculated with the following formulae Where m= modulation index & here 'm' is chosen as 1).

$$V_{dc} = \frac{2\sqrt{2}V_{LL}}{\sqrt{3}\,m} \quad (4)$$

The control block diagram of the parallel VSC is shown in Fig 6. From this control block diagram, we obtain the parameters K_2(Current error gain), K_3 (Voltage error gain) by performing stability analysis on transfer function G_3 . Here again PWM controller is modeled as Unity gain system (Kpwm = 1)

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The four transfer functions for the system is obtained as below

$$G_3=\frac{K_2\ K_3}{L_2S+(R_2\ +K_3+K_2K_3)}$$

$$G_4=\frac{K_2\ K_3}{L_2S+(R_2\ +K_3+K_2K_3)}$$

$$G_5=\frac{1-\alpha}{L_2S+(R_2\ +K_3+K_2K_3)}$$

$$G_6=\frac{L_2S+R_2\ +K_3-\beta K_3}{L_2S+(R_2\ +K_3+K_2K_3)}$$

Where G_3, G_4, G_5 and G_6 are the c1osed-loop transfer functions between the reference I^*_{sb} and i_{sb}, the DC-link voltage regulating current reference I^*_{dca} and i_{sb}, the voltage disturbance $V_{Lb2}V_{La}$ and i_{sb} , and current disturbance i_{Lb}-i_{b2}toi_{sb} respectively. a=1 &ß = (L_{2s} + R_2)/ (K_3* Kpwm + 1). The values used here in this paper are K_2 = 15, K_3= 10.

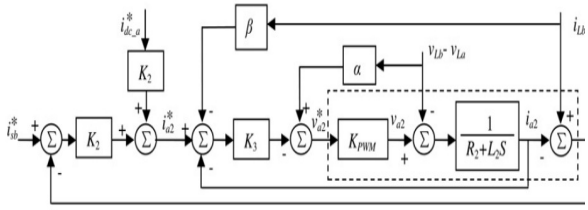

Fig 6 Control block diagram for parallel VSC

III. SIMULATION RESULTS

The scheme was verified using Matlab/SIMULINK 7.9.0 version. A supply voltage of 415 V, 50 Hz and the symmetrical load of 70KW was applied to the system. A harmonics load with an RL load (5Ω, 10 mH) is also switched to the system. The entire Simulink diagram is shown in Fig 7.

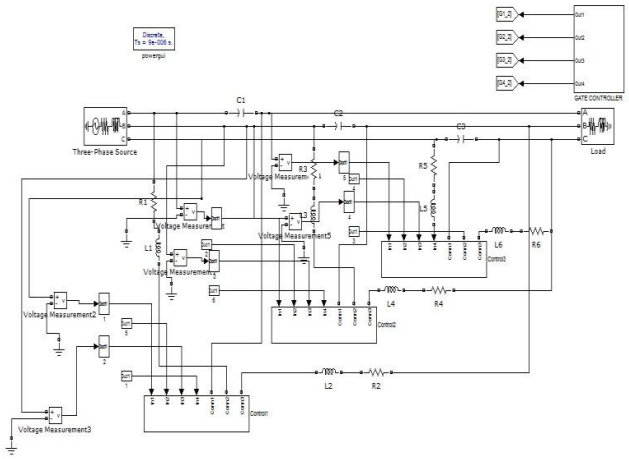

Fig 7 – Entire Simulink Model

The system is analyzed with three phase symmetrical fault during 0.1 s to 0.2 s. At the time period from 0.3 s to 0.4 s, a harmonics load is switched to the system . The supply voltage and current waveforms without UPQC are as below in fig 8(a) and (b) below.

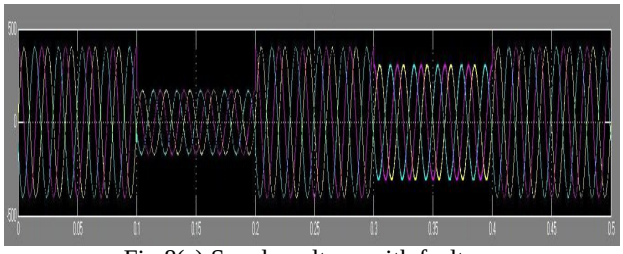

Fig 8(a) Supply voltage with fault

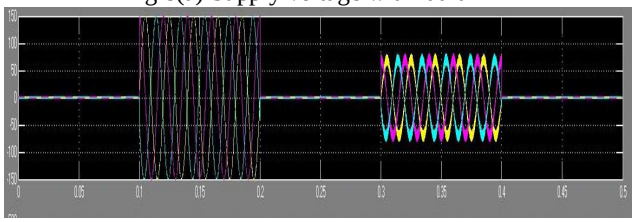

Fig 8(b) Supply current with fault

With the implementation of proposed UPQC, the faults should be rectified. The output waveforms are represented in Fig 9(a) & 9(b).

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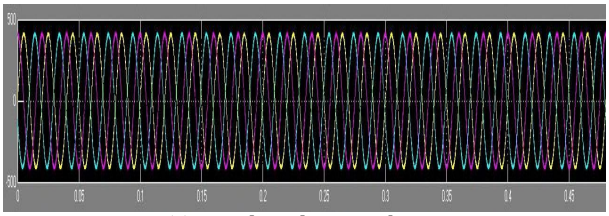

Fig 9(a) Supply voltage with UPQC

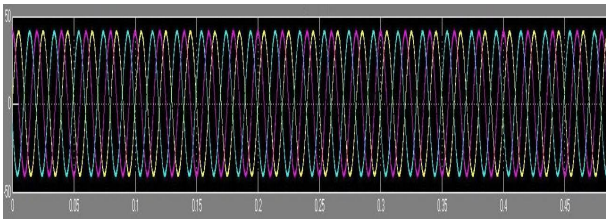

Fig 9(b) Supply current with UPQC

IV. CONCLUSION

The topology of a cross-phase-connected UPQC is introduced and two multi-loop control schemes are incorporated for the series and parallel VSC within the proposed UPQC. Extensive simulations are carried out to verify the practicability of the configuration and the effectiveness of the proposed control schemes under various operating conditions. It has been shown that the new control strategy for the UPQC is capable of protecting critical loads against voltage deviations, such as voltage imbalance, three-phase voltage sag/swell. Also, the UPQC with the proposed control can regulate the currents to be sinusoidal, balanced, and in phase with the positive phase sequence component of the supply voltage.

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