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Performance Evaluation of Asymmetrical Cascaded H-Bridge Multilevel Inverter

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ABSTRACT:A power electronic converters are becoming more and more popular for medium voltage & high power applications. To overcome the limitation of semiconductors current and voltage ratings in high power applications, multilevel inverter is often considered an effective solution. In addition, stepped waveform in the output of multilevel inverter has better harmonic spectrum than 2-level inverter in low switching frequencies. So, in recent years multilevel inverters have gained great interest in industry. Among the different solutions available for multilevel converters, the cascaded H-Bridge multilevel inverter are modular in nature and its asymmetric topologies allow to generate more voltage levels with less number of semiconductors and thus increase of output performance and system reliability. For these reasons, this kind of topology has attracted a lot of attention both from the customers and manufacturers view.This paper presents an asymmetrical cascaded H-Bridge multilevel inverter in three phase configuration using fixed frequency level shifted carrier based pulse width modulation technique feeding a three phase squirrel cage induction motor. This new control scheme is applied to 7, 9, 15 and 27 level asymmetrical cascaded H-Bridge multilevel inverter. Simulation using MATLAB/SIMULINK is done to verify the performance of all levels of an asymmetrical cascaded H-Bridge multilevel inverter.

KEYWORDS: Multilevel Inverter (MLI), Asymmetrical Cascaded H-Bridge Multilevel Inverter(ACMLI), Level Shifted Carrier Based Sinusoidal Pulse Width Modulation (LSCPWM) Technique.

I.INTRODUCTION

Multilevel power conversion technology is a very rapidly growing area of power electronics with a good potential for further development [1]-[7]. The most attractive applications of this technology are in the medium voltage (2.3-13.8 KV)and high power range (0.2-40 MW), and include motor drives, power distribution, power quality and power conditioning applications [2]-[5]. Ordinary two level inverters cannot be used for high power and high voltage applications because of limitation in power handling capability and rating of the semiconductor devices [6]-[8]. To overcome the limited semiconductor voltage and current ratings, some kind of series and/or parallel connection will be necessary thereby allowing greater working voltages to be reached, which in turn increases the power they are able to handle [9]. Due to their ability to synthesize waveforms with a better harmonic spectrum and attain higher voltages, multi-level inverters are receiving increasing attention in the past few decades. The three most important topologies have been proposed for multilevel inverters [5]-[11]: diode-clamped (neutral-clamped); capacitor-clamped (flying capacitors) and cascaded H-Bridge Multilevel inverter with separate dc sources.Diode clamped requires more no of diodes and flying capacitor has capacitor balancing problem. In addition, several other topologies have been proposed in the literature [5], [7]. The cascaded H-bridge multilevel inverters having more no of advantages such as modular structure and less no of components required compare to other topologies. It is one of the topologies proposed for drive applications which meet the requirements such as high power rating with reduced THD and switching losses.

For higher-level operation, cascaded H-Bridge multilevel inverter are preferred but major disadvantage is requirement of multiple dc-sources, which is not feasible in many applications.With an aim to reduce the number of dc sources required for the cascaded H-Bridge multilevel inverter, a focuses on asymmetrical cascaded H-Bridge multilevel inverter that uses unequal dc sources in each phase to generate a three- phase equal step multilevel output [15]. There are many modulation techniques are discussed in the literature to control the multilevel inverter such as selective

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harmonic elimination [5], space vector modulation [7], carrier-based sinusoidal pulse width modulation [9], etc. In this paper, level shifted carrier-based SPWM technique is used for ACMLI because of its advantages of simple logic and easy implementation.

II.SYMMETRICAL & ASYMMETRICAL CASCADED H-BRIDGE MULTILEVEL INVERTER

A relatively new power converter structure, cascaded H-Bridge multilevel inverters with separate DC sources is introduced here. This new converter can avoid extra clamping diodes or voltage balancing capacitors. Fig. 1 shows the basic structure of the cascaded H-Bridge multilevel inverter with separate DC sources for three phase configuration. The AC terminal voltages of different level inverters are connected in series. The phase output voltage is synthesized by the sum of inverter outputs. Each single-phase full bridge inverter can generate three level outputs, +Vdc, 0, and -Vdc. This is made possible by connecting the DC sources sequentially to the AC side via the four semiconductor power devices. Fig. 2 illustrates the voltage polarities (positive, zero and negative polarities) for the first H-bridge cell according to the switching states.

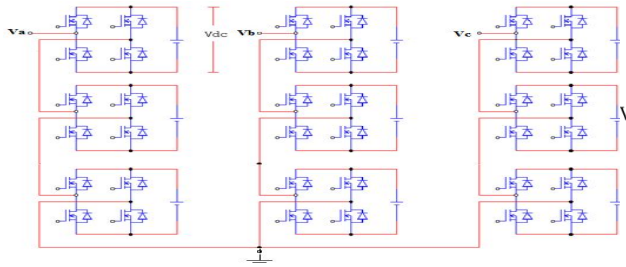

Fig.1 Three phase Y-configured ACMLI

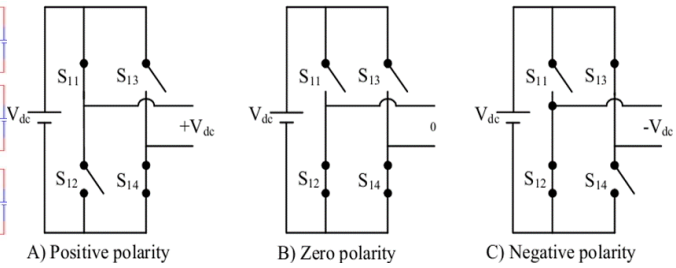

Fig. 2 Output voltage polarities for the first H-bridge cell

This method introduces the idea of using separate DC sources to produce an AC voltage waveform which is nearly sinusoidal. Each H-bridge inverter is connected to its own DC source. By cascading the output voltage of each H-bridge inverter, a stepped voltage waveform is produced. For many applications it is difficult to use separate dc sources and too many dc sources will require many long cables and could lead to voltage imbalance among the dc sources. To reduce the number of dc sources required for the cascaded H-bridge multilevel inverter, an asymmetrical topology is proposed which uses lesser number of bridges and dc sources. This scheme therefore provides the capability to produce higher voltages at higher speeds with low switching frequency which has inherent low switching losses and high converter efficiency.

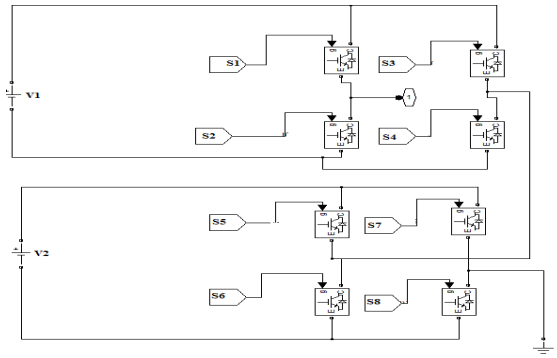

Fig. 3 One phase leg of an ACMLI for 7 and 9-level

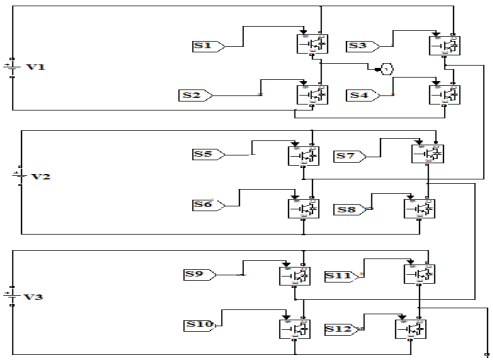

Fig.4 One phase leg of an ACMLI for 15 and 27-level

In ACMLI, DC voltage with ratio binary and ternary are the most popular. In binary progression within H-Bridge inverters, the DC voltages having ratio 1:2:4:8….:2N-1 and the maximum voltage output would be (2N-1) Vdc and the voltage levels will be (2N+1-1). While in the ternary progression the amplitude of DC voltages having ratio 1:3:9….:3

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N-1 and the maximum output voltage reach to ((3N-1)/2) Vdc and the voltage levels will be 3N, where N is the no. of H-Bridges. Fig.3 and Fig. 4 shows the power circuit of an asymmetrical cascaded H-Bridge multilevel inverter. For clarity of the figure, only one phase leg is shown in the figure. For 7 and 9-level ACMLI only two H-Bridges are needed with binary and ternary ratio respectively as shown in Fig. 3 and for 15 and 27-level ACMLI three H-Bridges are needed with binary and ternary ratio respectively as shown in Fig. 4. In this topology, each cell has separate dc link voltages which are in different ratios for obtaining different levels. Each H-Bridge cell may have positive, negative or zero voltage. Final output voltage is the sum of all H-bridge cell voltages and is symmetric with respect to neutral point, so the number of voltage levels is odd. The output voltage of each H-Bridge cell for both binary and ternary ratio are given in Table. 1 and Table. 2 respectively.

Table. 1 Output voltage of each H-Bridge cell for 7 and 15-level

Output Voltage of each cell	**Value**	**States**	
		Switches	**Polarity**
V_1 (H-Bridge cell 1)	$+V_{dc}$	S_1-S_4 ON	P
	0	S_2-S_4 ON	Z
	$-V_{dc}$	S_2-S_3 ON	N
V_2 (H-Bridge cell 2)	$+2V_{dc}$	S_5-S_8 ON	P
	0	S_6-S_8 ON	Z
	$-2V_{dc}$	S_6-S_7 ON	N
V_3 (H-Bridge cell 2)	$+4V_{dc}$	S_9-S_{12} ON	P
	0	S_{10}-S_{12} ON	Z
	$-4V_{dc}$	S_{10}-S_{11} ON	N

Table. 2 Output voltage of each H-Bridge cell for 9 and 27-level

Output Voltage of each cell	**Value**	**States**	
		Switches	**Polarity**
V_1 (H-Bridge cell 1)	$+V_{dc}$	S_1-S_4 ON	P
	0	S_2-S_4 ON	Z
	$-V_{dc}$	S_2-S_3 ON	N
V_2 (H-Bridge cell 2)	$+3V_{dc}$	S_5-S_8 ON	P
	0	S_6-S_8 ON	Z
	$-3V_{dc}$	S_6-S_7 ON	N
V_3 (H-Bridge cell 2)	$+9V_{dc}$	S_9-S_{12} ON	P
	0	S_{10}-S_{12} ON	Z
	$-9V_{dc}$	S_{10}-S_{11} ON	N

Seven level asymmetrical cascaded H-Bridge multilevel inverter consists of two H-bridges. The dc voltage having ratio 1:2 V_{dc} and the maximum output voltage is $3V_{dc}$. The switching states of 7-level output voltage is shown in Table. 3.

Table. 3 Switching states of 7-level output voltage

$V_{o/p}$	V_1	V_2	$V_{o/p}$	V_1	V_2
$-3\ V_{dc}$	N	N	$+3\ V_{dc}$	P	P
$-2\ V_{dc}$	Z	N	$+2\ V_{dc}$	Z	P
$-V_{dc}$	N	Z	$+\ V_{dc}$	P	Z
0	Z	Z			

Nine level asymmetrical cascaded H-Bridge multilevel inverter also consists of two H-bridges. But the dc voltage having ratio 1:3 Vdc and the maximum output voltage is 4Vdc. The switching states of 9-level output voltage is shown in Table. 4.

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Table. 4 Switching states of 9-level output voltage

$V_{o/p}$	V_1	V_2	$V_{o/p}$	V_1	V_2
-4 V_{dc}	N	N	+4 V_{dc}	P	P
-3 V_{dc}	Z	N	+3 V_{dc}	Z	P
-2 V_{dc}	P	N	+2 V_{dc}	N	P
-V_{dc}	N	Z	+ V_{dc}	P	Z
0	Z	Z			

Fifteen level asymmetrical cascaded H-Bridge multilevel inverter consists of three H-bridges. The dc voltage having ratio 1:2 Vdc and the maximum output voltage is 7Vdc. The switching states of 15-level output voltage is shown in Table. 5.

Table. 5 Switching states of 15-level output voltage

$V_{o/p}$	V_1	V_2	V_3	$V_{o/p}$	V_1	V_2	V_3
-7 V_{dc}	N	N	N	+7 V_{dc}	P	P	P
-6 V_{dc}	Z	N	N	+6 V_{dc}	Z	P	P
-5 V_{dc}	P	N	N	+5 V_{dc}	N	P	P
-4 V_{dc}	Z	Z	N	+4 V_{dc}	Z	Z	P
-3 V_{dc}	N	N	Z	+3 V_{dc}	P	P	Z
-2 V_{dc}	Z	N	Z	+2 V_{dc}	Z	P	Z
-V_{dc}	N	Z	Z	+V_{dc}	P	Z	Z
0	Z	Z	Z				

Twenty-seven level asymmetrical cascaded H-Bridge multilevel inverter also consists of three H-bridges. But the dc voltage having ratio 1:3 Vdc and the maximum output voltage is 13Vdc. The switching states of 27-level output voltage is shown in Table. 6.

Table. 6 Switching states of 27-level output voltage

$V_{o/p}$	V_1	V_2	V_3	$V_{o/p}$	V_1	V_2	V_3
-13 V_{dc}	N	N	N	+13 V_{dc}	P	P	P
-12 V_{dc}	Z	N	N	+12 V_{dc}	Z	P	P
-11 V_{dc}	P	N	N	+11 V_{dc}	N	P	P
-10 V_{dc}	N	Z	N	+10 V_{dc}	P	Z	P
-9 V_{dc}	Z	Z	N	+9 V_{dc}	Z	Z	P
-8 V_{dc}	P	Z	N	+8 V_{dc}	N	Z	P
-7 V_{dc}	N	P	N	+7 V_{dc}	P	N	P
-6 V_{dc}	Z	P	N	+6 V_{dc}	Z	N	P
-5 V_{dc}	P	P	N	+5 V_{dc}	N	N	P
-4 V_{dc}	N	N	Z	+4 V_{dc}	P	P	Z
-3 V_{dc}	Z	N	Z	+3 V_{dc}	Z	P	Z
-2 V_{dc}	P	N	Z	+2 V_{dc}	N	P	Z
-V_{dc}	N	Z	Z	+V_{dc}	P	Z	Z
0	Z	Z	Z				

III.CARRIER BASED SINUSOIDAL PWM TECHNIQUE

This highly conventional technique is based on the comparison of a sinusoidal reference with carrier signals which are usually selected triangular and modified in phase or vertical positions to reduce the output voltage harmonic content. Due to simplicity and popularity of this technique, it will be analysed in this thesis in details and will be used as the modulator of the multilevel topologies.

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The carrier-based modulation schemes for multilevel inverters can be generally classified into two categories: phase-shifted and level-shifted modulations. Both modulation schemes can be applied to the asymmetrical cascaded H-bridge multilevel inverters. Total harmonics distortion of phase-shifted modulation is higher than the level-shifted modulation. Therefore we have considered level-shifted modulation. An m-level proposed multilevel inverter using level shifted multicarrier modulation schemes requires (m-1) triangular carriers, all having the same frequency f_c and amplitude A_c. The (m-1) triangular carriers are vertically disposed such that the bands they occupy are adjacent to each other. The reference waveform has amplitude of A_m and frequency of $f_m$and it is placed in the middle of the carriers. The reference wave is continuously compared with each of the carrier signals. There are three types of level shifted carrier-based PWM techniques as follows:

A. Phase Disposition Technique (PD)

The vertical offset of carriers for 7-level of ACMLI with PD technique is illustrated in Fig. 5. It can be seen that all carriers are adjacent to each other with same phase and the reference sine wave is placed in the middle of the carriers. Here, one sinusoidal wave is compared with six triangular signals. Similarly, for other levels one sinusoidal wave is compared with (m-1) triangular signals where m is the no. of levels.

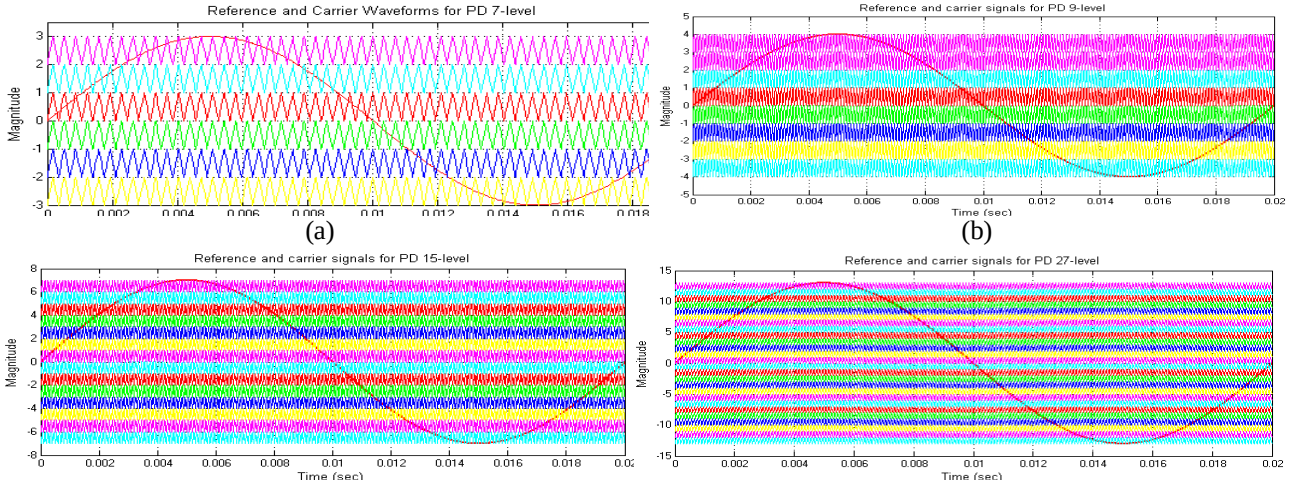
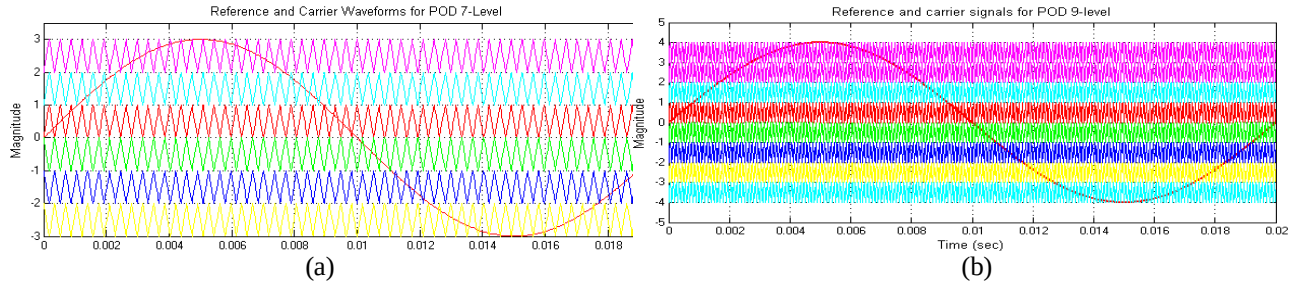


Fig. 5 Reference and carrier signals for PD technique: (a) 7-level (b) 9-level (c) 15-level (d) 27-level

B. Phase Opposition Disposition Technique (POD)

The vertical offset of carriers for all levels of ACMLI with POD technique is illustrated in Fig. 6. It can be seen that they are divided equally into two groups according to the positive/negative average levels. In this type the two groups are opposite in phase with each other while keeping in phase within the group. The reference wave is placed in the middle of the carriers.Here, one sinusoidal wave is compared with six triangular signals. Similarly, for other levels one sinusoidal wave is compared with (m-1) triangular signals where m is the no. of levels.



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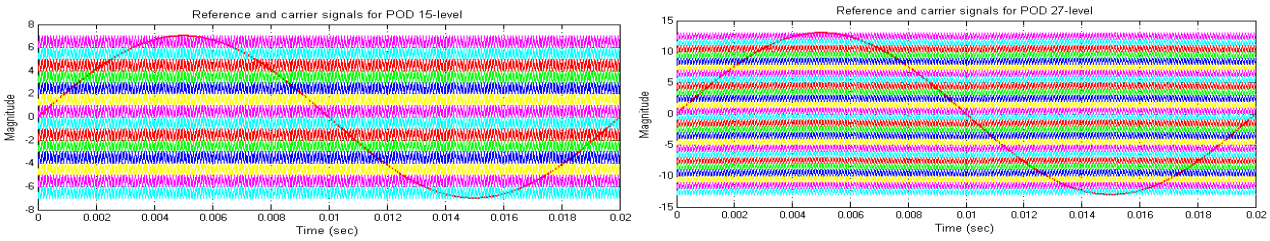
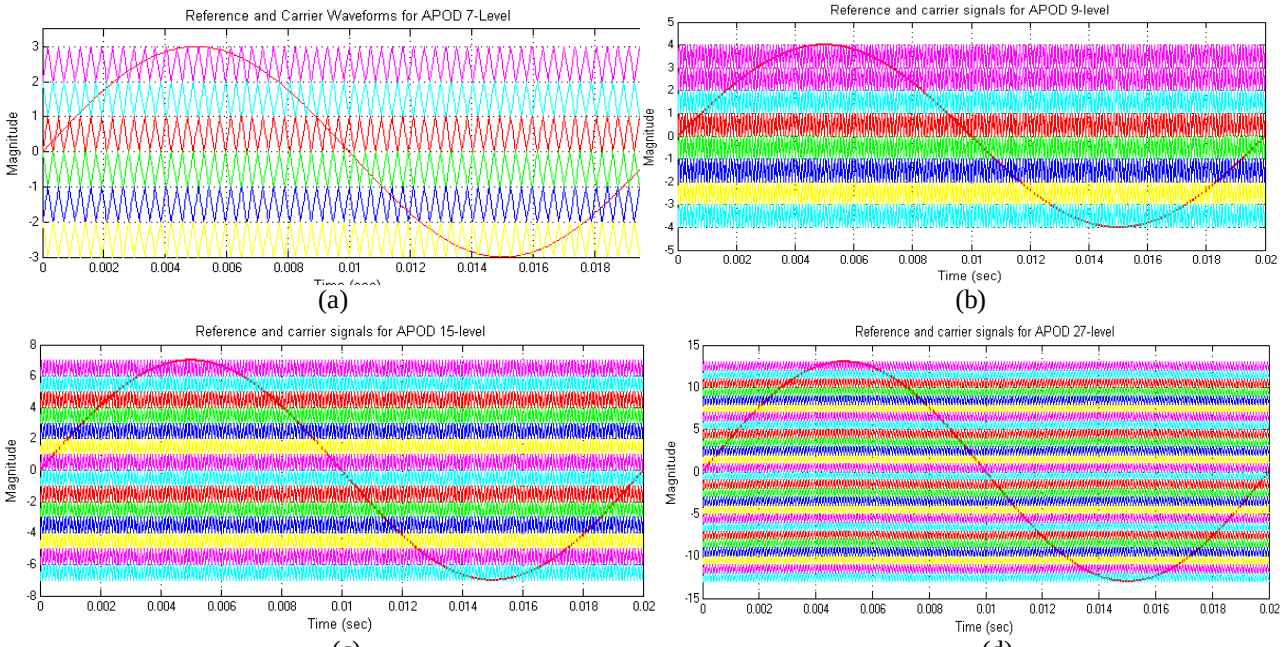


(c) (d)

Fig. 6 Reference and carrier signals for POD technique: (a) 7-level (b) 9-level (c) 15-level (d) 27-level

C. Alternative Phase Opposition Disposition Technique (APOD)

The vertical offset of carriers for all levels of ACMLI with APOD technique is illustrated in Fig. 7. In this technique, all carriers are opposite in phase with each other and the reference wave is placed in the middle of the carriers. Here, one sinusoidal wave is compared with six triangular signals. Similarly, for other levels one sinusoidal wave is compared with (m-1) triangular signals where m is the no. of levels.



(a) (b)

(c) (d)

Fig. 7 Reference and carrier signals for APOD technique: (a) 7-level (b) 9-level (c) 15-level (d) 27-level

IV.STUDY CASE IMPLEMENTED IN MATLAB

The simulation of three phase 7, 9, 15 and 27-level asymmetrical cascaded H-Bridge multilevel inverter is carried out using MATLAB/SIMULINK as shown in Fig 8. Here the subsystem for pulse generator is modeled where one reference wave (sine wave) and (m-1) carrier signals (triangular wave) are taken. First ((m-1)/2) triangular wave is applied across the positive half cycle of the sine wave and the second ((m-1)/2) triangular wave is applied across the negative half cycle of the sine wave.

Based on the concepts explained in modulation techniques, eight pulses are generated for 7 & 9-level and twelve pulses are generated for 15 & 27-level. These pulses are given to the switches in one phase leg of an ACMLI. Similarly the pulses are generated for remaining two phases, just by changing phase shifting angle of modulating signal by 120

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degrees. Fig 9: represents the logic circuit of a 7-level. Based on this concept other levels of logic circuit are also designed.

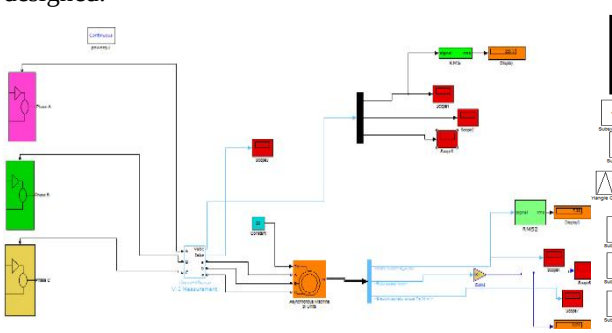

Fig.8 Simulink diagram of an ACMLI

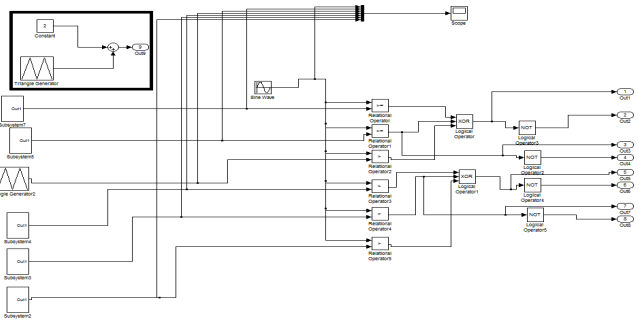

Fig. 9 Logic circuit

V. RESULTS AND DISCUSSION

The performance is analyzed for all levels of ACMLI with different level shifted SPWM technique feeding a three phase squirrel cage induction motor. Also the harmonic analysis is being carried out for all levels of ACMLI with different SPWM technique i.e., PD, POD, APOD.All the resulting waveforms are discussed here in detail and it is clear that the THD is reduced by increasing the levels of ACMLI. So it can be concluded that the higher level of ACMLI gives low THD. For comparison of all levels of ACMLI fed induction motor drive, it is important to examine few parameters of the system. The parameters & ratings of a three phase squirrel cage induction motor and the system are specified in Table. 7.

Table. 7 Parameters & ratings of a three phase induction motor and the system

Voltage (L-L) V_{L-L}	400 V	Stator Resistance R_s	1.405Ω
Frequency f	50 Hz	Stator Leakage Inductance L_{ls}	5.839 mH
Nominal Power of Motor P_o	10 HP (7.5KW)	Rotor Resistance R_r	1.395 Ω
Rated Speed N_r	1440 rpm	Rotor Leakage Inductance L_{lr}	5.839 mH
Rated Current I	10.825 Amp	Mutual Inductance L_m	172.2 mH
Load Torque T_l	20 N-m	Moment of Inertia J	0.089 kg-m^2
No. of Poles P	4	Carrier Frequency fcr	10 KHz

The output voltage waveform for phase A of 7, 9, 15 and 27-level ACMLI with three phase squirrel cage induction motor as a load using LSCPWM technique is shown in Fig. 10-13. It can be observed that there are few notches in the voltage waveform and 27-level voltage waveform is closed to sinusoidal waveform as shown in Fig. 13.

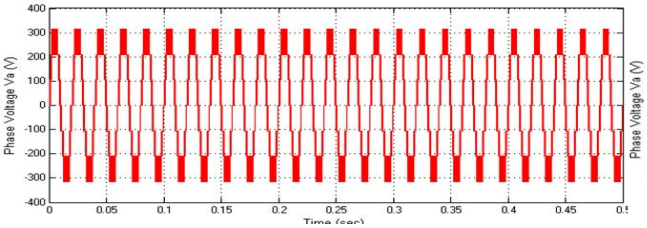

Fig. 10 7-level of an ACMLI phase voltage V_a

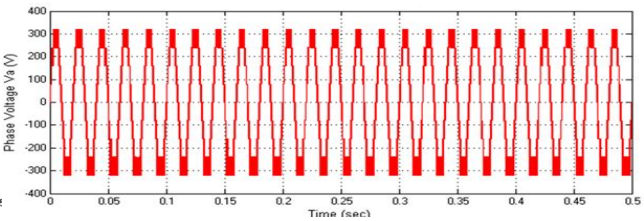

Fig. 11 9-level of an ACMLI phase voltage V_a

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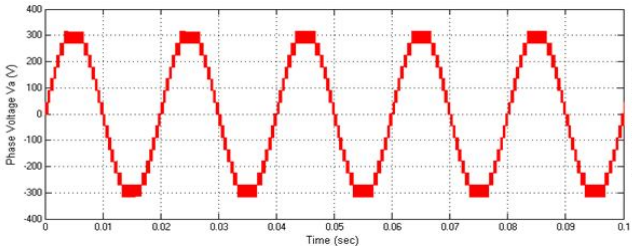

Fig. 12 15-level of an ACMLI phase voltage V_a

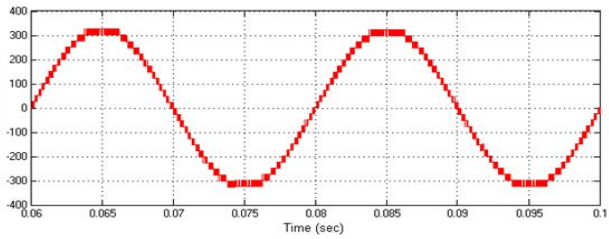

Fig. 13 27-level of an ACMLI phase voltage V_a

The three phase stator current are much closer to sinusoidal as shown in Fig. 14. The speed response of the three phase squirrel cage induction motor driven by the proposed converter has been shown in Fig.15. The peak overshoot is 1600 rpm and starts to settle down after peak value. At time 0.15 sec it completely settled down to rated speed 1440 rpm. In steady state, a small speed ripple is introduced due to harmonics of the output voltage, specifically the fifth and seventh harmonics. Similarly the torque shown in Fig. 16 contains some ripples because of harmonics. From Fig.17 which represents the harmonic spectrum, it can be observed that the total harmonic distortion (THD) of the 27-level ACMLI using APOD technique for phase voltage A is 4.15% at a modulation index of 1 and within limit prescribed by power quality standards.

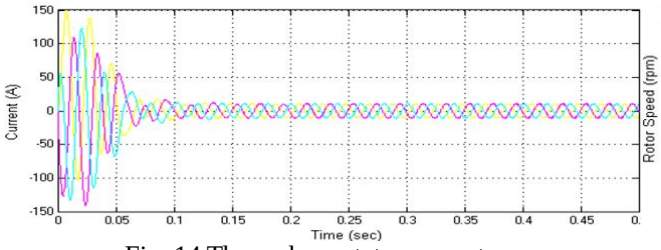

Fig. 14 Three phase stator current

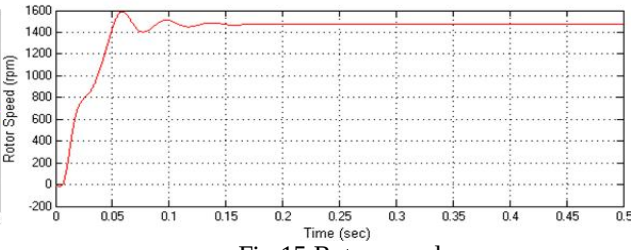

Fig.15 Rotor speed

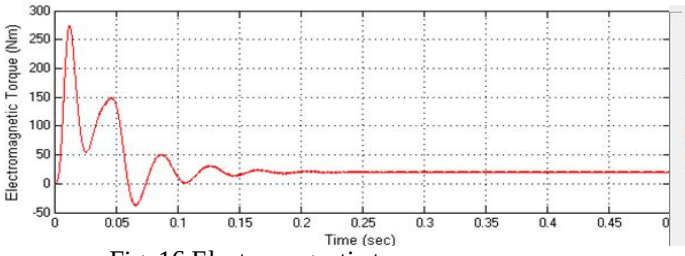

Fig. 16 Electromagnetic torque

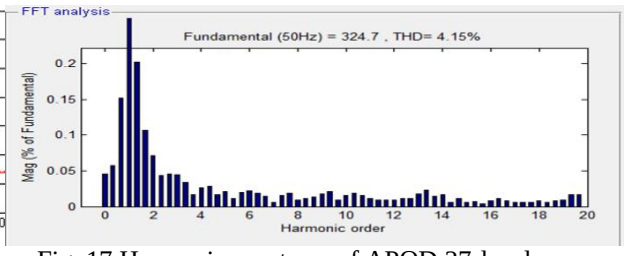

Fig. 17 Harmonic spectrum of APOD 27-level

ACMLI

The comparison between all the levels of ACMLIis shown below in Table. 8.Performance indices like THD%, (indicating the amount of DC bus utilization), Crest Factor (CF) and Form Factor (FF) related to power quality issues have been evaluated, presented and analysed. The results of multilevel inverter systems are compared with different sinusoidal pulse width modulation techniques. It is observed that the total harmonic distortion produced by the 27-Level is 4.15%which is less than the other levels of ACMLI and it is also observed that by using APOD technique we get less THD by comparing other techniques.

Table. 8 Performance comparison of all levels of ACMLI

Levels	No. of Switches	No. of DC Sources	THD% of Phase Voltage Va			V_{max} (V)	V_{rms} (V)	V_{avg} (V)	Form Factor (F.F.)	Crest Factor (C.F.)
			PD	POD	APOD					
7	8	2	17.76	18.05	17.72	105+210 = 315	226.5	200.2	1.1313	1.3907
9	8	2	15.27	15.55	15.05	80+240 = 320	227.3	203.4	1.1175	1.4078

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15	12	3	7.78	7.79	7.72	45+90+180 = 315	223.5	200.1	1.1169	1.4094
27	12	3	4.16	4.18	4.15	25+75+225 = 325	230.1	206.4	1.1148	1.4124

VI.CONCLUSION

The lower amount of disturbances is one of the more frequently mentioned advantages for multilevel inverters. It seems that the biggest reason for using multilevel inverters is to lower the THD so that less filters needs to be used. Compared to the NPCMLI and CCMLI, the CMLI requires fewer components, every voltage level requires the same amount of components. However, the numbers of sources are higher, for the phase-leg to be able to create a number of m voltage levels.To reduce the number of dc sources required for the cascaded H-bridge multilevel inverter, an asymmetrical topology is proposed which uses lesser number of bridges and dc sources. This scheme therefore provides the capability to produce higher voltages at higher speeds with low switching frequency which has inherent low switching losses and high converter efficiency.The THD of the Phase Voltage of all levels of ACMLI is studied under different level shifted carrier based sinusoidal pulse width modulation techniques such as PD, POD, and APOD and the less THD is observed for 27 level ACMLI and it also concluded that APOD is the best technique.

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