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Performance Evaluation of Digital CMOS Circuits Using Complementary Pass Transistor Network

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***Abstract*—** An important issue in the design of VLSI Circuits is the choice of the basic circuit approach and topology for implementing various logic and arithmetic functions such as adders and multipliers. Complementary Pass-transistor Logic (CPL) is the approach to reduce the physical capacitances in a digital circuit and in this way lower the power consumption. Charge-recovery circuitry has the potential to reduce dynamic power consumption in digital systems with significant switching activity. The overall energy-efficiency of charge-recovery circuitry therefore depends on the rate at which transitions occur, yielding an inverse relationship between energy consumption and clock period.This paper mainly focuses on Boost Logic, a charge recovery circuit family that can operate efficiently at clock frequencies in excess of 1 GHz. Complementary Pass-transistor Boost Logic(CPBL) is a low-power charge recovery logic structure powered by 2-phase non-overlap alternating power clocks PC and ~PC and requires no DC power supply. To achieve high energy efficiency, Boost Logic relies on a combination of aggressive voltage scaling, and charge-recovery techniques. In order to achieve low power in adders (Full Adder, Ripple Carry Adder), Multiplexer and Multiplier has been designed using CPBL. The power efficiency obtained using CPBL is 16% lower than CPAL (Complementary Pass-transistor Adiabatic Logic). Low power circuits are designed using CPBL is simulated using Tanner EDA 15.1.

Keywords— Low-power, Charge recovery logic, CPL ,CPBL, CPAL, Adders, Tanner EDA, power clock.

I. INTRODUCTION

Main objectives of most of the system level or circuit design are high performance and power optimization. For high performance system design, propagation delay minimization plays an important role. Basically size, cost, performance and power consumption are the crucial issues in low power portable battery operated system design. Excessive power dissipation which overheats thereby degrading the performance and lifetime is not at all affordable. Energy consumption being an important constraint for battery life estimation, VLSI based low power design of dedicated multimode signal conditioning integrated circuit is desirable. Modern systems consist of digital realization of analog processes and this helps to design system with high precision, high signal to noise ratio, repeatability and flexibility. DSP systems can be realized with custom designed hardware circuits or ultra-low power high performance programmable processors fabricated using VLSI circuit technology.

II.N-TYPE Vs P-TYPE TRANSISTORS

Motivation to reduce energy consumption of logic circuits comes from increasing difficulties in removing heat from high speed VLSI circuits. The importance of reducing power dissipation in digital systems is increasing as the range and complexity of applications in portable and embedded computing continues to increase. System-level issues such as battery life, weight, and size are directly affected by power dissipation. A trend into reducing power dissipation of the digital systems only serves to improve the performance and capabilities of these systems.

The power dissipation is a critical concern in the design of VLSI circuits with increasing package density and working speed. Also the energy consumption of battery-driven systems is above all problem to be considered. Many low power design methods have been developed to reduce CMOS digital circuit's power consumption. However the adiabatic circuit is an attractive way to obtain extreme low power level which conventional CMOS digital circuit can't reach. At present time, lots of digital systems are targeted at portable, battery-operated systems, so power dissipation is one of the primary design constraints.

To reduce the power dissipation, the circuit designer can minimize the switching events, decrease the node capacitance, reduce the voltage swing, or apply a

combination of these methods. In all these cases, the energy drawn from the power supply is used only once before being dissipated. To increase the energy efficiency of the logic circuit, other measures can be introduced for recycling the energy drawn from the power supply. A novel class of logic circuits called Adiabatic Logic offers the possibility of further reducing the energy dissipated during switching events, and the possibility of recycling or reusing, some of the energy drawn from the power supply.

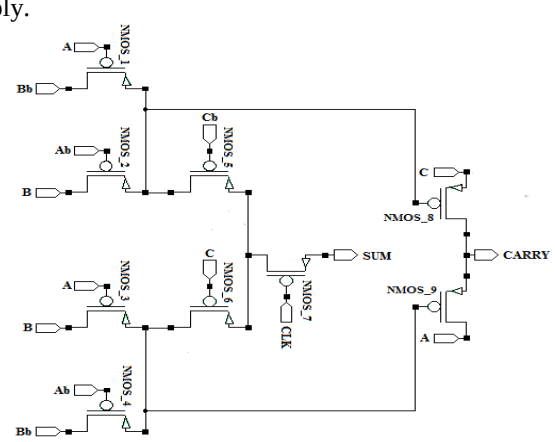

Fig 1.PMOS Full Adder

Recently, a novel approach to reduce power dissipation in digital circuits was proposed, which is to be used and verified in many digital applications. The approach, called adiabatic logic design, utilizes clocked ac power to slowly charge the node capacitances and then partially recover the energy associated with that charge. The term adiabatic is typically used to describe thermodynamic process that has no energy exchange with the environment, and therefore no energy loss in the form of heat.

Adiabatic digital circuits have the ability to recover energy once committed in computation and make it available for recycling. Due to the trend of increasing clock frequencies and transistor count, power demands new System-on-Chip designs will continue to grow. Adiabatic logic style has emerged as a promising approach to achieve ultra-low power without sacrificing noise immunity and driving ability. Adiabatic circuits are low power circuits which use "reversible logic" to conserve energy.

Adiabatic logic is a low–power circuit design approach where the signal energy stored on a capacitor may be recycled instead of dissipated as heat. Power dissipation can be avoided if the capacitor is slowly charged with a voltage ramp. It is possible to recover this charge back into the power source by discharging the capacitor to a down–ramping supply. Adiabatic principles, together with charge reuse by redistribution, can be utilized for power saving in interconnects.

Adiabatic logic is an attractive low power approach by utilizing AC voltage supplies (power clocks) to recycle the energy of circuits instead of being dissipated as heat. Adiabatic circuits are work on the principal of adiabatic charging and discharging by which energy is recycled from output nodes instead of discharging it to ground. Conventional CMOS circuits achieve a logic='1' or logic='0' by charging the load capacitor to supply voltage V_{dd} and discharging it to ground respectively. Thus every time a Charge-discharge cycle occurs an amount of energy equal to CV2 is dissipated. Unlike the conventional CMOS circuits, in adiabatic circuits energy is recycled. Instead of discharging the capacitor to ground, the charge is discharged to the power supply.

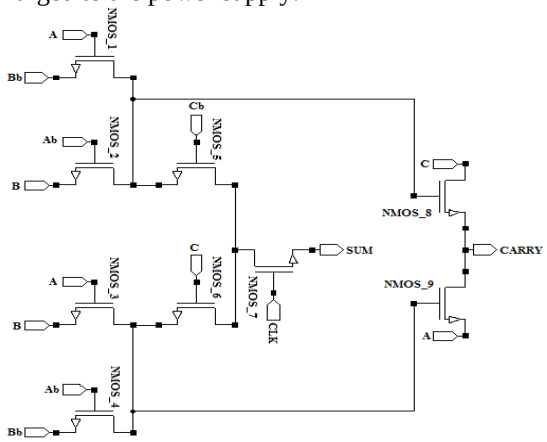

Fig 2.NMOS Full Adder

Since the charge has to be discharged to supply, the supply in adiabatic circuits is a time varying one called the power clock. It has been observed that among the different waveforms for charging or discharging the load capacitor, a ramp is more efficient and as such trapezoidal power clocks have been used in many adiabatic circuit styles. Many adiabatic logic circuits which dissipate less power than static CMOS logic circuits have been introduced as a promising approach in low power circuit design.

Field Programmable Gate Arrays have traditionally been configured by hardware designers using specific so called Hardware Design Languages (HDLs). There are already few such languages available offering different levels of abstraction but the most important ones are Verilog HDL(VHDL) and Very High Speed Integrated Circuits (VHSIC).

III.CHARGE RECOVERY

Charge-recovery circuitry has the potential to reduce dynamic power consumption in digital systems with significant switching activity. To keep energy consumption to a minimum, Charge-recovery circuitry is typically designed so that it maintains low voltage drops across device channels, while recovering the charge supplied to it every clock cycle. The overall energy-efficiency of charge-recovery circuitry therefore depends on the rate at which transitions occur, yielding an inverse relationship between energy consumption and clock period. Relying on this energy/latency tradeoff, Charge-recovery circuitry can operate with energy consumption below, the fundamental limit of static CMOS.

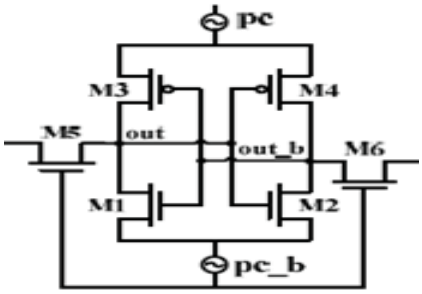

Fig 3. Charge Recovery Logic.

Early research on Charge-Recovery Logic design focused on micro pipelined dynamic circuits with multiple (four or more) clock phases for recovering charge. These clock phases were generated by resonating the parasitic capacitance of the circuitry through the introduction of inductors. To maximize the efficiency of recovery, the inductors were chosen so that the resulting tank system resonates at the target clock frequency. In these early multiphase designs, the resulting complexity of the recovery mechanisms was considerable, especially in the case of the so-called reversible designs, which theoretically offer the greatest energy saving potential. Moreover, the synchronization of multiple clock phases was impeding high-speed operation.

IV. Complementary Pass Transistor Logic

Low power techniques are of great importance in VLSI design applied for digital electronics, especially the portable devices. Several techniques have been developed to achieve the goal of low power dissipation. Voltage scaling is one of the most effective methods to reduce dynamic power consumption in digital system, as the energy consumed when charging and discharging a capacitive load C across a voltage difference V grows quadratic ally with V.

Charge Recovery Logic (CRL) is one of the most promising methods to achieve low power dissipation in digital systems with significant switching activities. The CRL structure is powered by power clocks, the sinusoidal signals produced by RLC resonant circuit, with which charges are recycled to power supply instead of flowing to the ground and being consumed.

A new Charge Recovery Logic structure called Complementary Pass-transistor Boost Logic (CPBL) is proposed, fully powered by 2-phase non-overlap alternating power clocks pc and ~pc, energy dissipates only on the parasitic resistance of the transistors working in linear region which is different from the proposed Boost Logic that DC power supply is still necessary. Each CPBL gate consists of two parts working in mutually exclusive intervals: the logical evaluation stage (Logic) and charge-recovering amplification stage (Boost). Logic stage is implemented by complementary pass-transistor network, while the Boost stage consists of a pair of cross-coupled inverters connected to the pc and ~pc.

The operation of CPBL gate is explained in Section 4.1 in detail. Also another charge recovery structure CPAL involved with pass-transistor network has been proposed. However, it suffers from some problems, such as low operation frequency and the need of transform circuit to produce particular power clock waveforms. The CPBL has relieved these problems and retains the merit of energy saving in the meanwhile.

A. CPBL STRUCTURE

Fig4. shows the basic structure of Complementary Pass-transistor Boost Logic (CPBL). Each CPBL gate consists of two parts: the complementary pass-transistor network which acts as the logical evaluation part, the ‘‘Logic’’ and a pair of cross-coupled inverters connected to complementary power clocks pc and ~pc which acts as the charge recovery amplification part, the ‘‘Boost’’. They work in two mutually exclusive intervals which will be referred to as Logic and Boost stages.

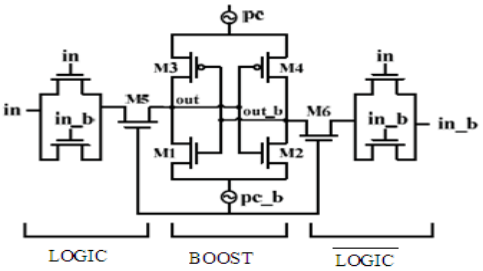

Fig 4. CPBL Structure

B.CPBL OPERATION

Each CPBL gate operates in two stages, Logic and Boost. When Logic evaluates, Boost does not drive the outputs and vice versa. The voltage swing of power clock is from 0 to V_{DD}.

During the Logic stage, power clock pc and ~pc are in low half cycle and high half cycle respectively. As such, Boost stage is in cut-off and the clocked transistors M5 and M6 turn on, evaluated logic values can be transferred to output nodes. The complementary pass-transistor network charges the out2 to approximately V_{DD}-V_{TH} and discharges the out2 to the GND and there is a little voltage difference achieved across the output nodes by the end of the Logic stage. The Schematic design for the CPBL AND gate as shown in the following figure.

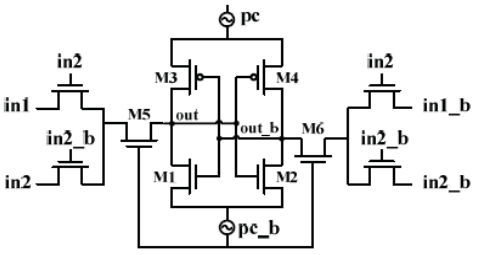

Fig 5. CPBL AND gate

This work presents a new Charge Recovery Logic structure, the Complementary Pass-transistor Boost Logic (CPBL) which is capable of achieving considerable low power dissipation while operating at multi-MHz CPBL consists of two parts: the complementary pass-transistor network and 4-Transistor Boost stage, fulfilling the logical evaluation and signal amplification respectively. It is fully powered by 2-phase alternating sinusoidal power clocks pc and ~pc produced by RLC resonant circuit.

V.RESULTS AND DISCUSSION

A. SCHEMATIC SIMULATION

In this work, the Schematic design of Digital CMOS circuits using Complementary Pass Transistor Logic (CPL) is designed and simulated in the S-Edit. The power consumption is estimated by using the T-spice and their corresponding simulated waveform results are obtained in W-Edit.

Transistor count of CPAL circuits are considerably less than the another techniques of Adiabatic Logic Design. CPAL circuits have more efficient energy transfer and recovery, because the non-adiabatic energy loss of output Loads has been completely eliminated by using complementary pass-transistor logic for evaluation and transmission gates for energy recovery. Complementary pass transistor logic concept reduces the complexity of circuit.

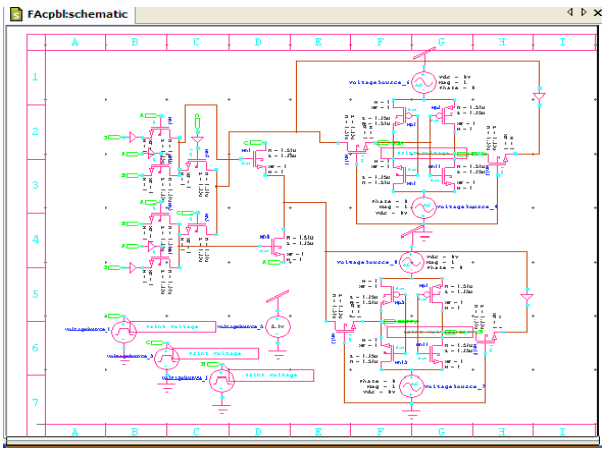

Fig 6. Schematic view of FULL ADDER

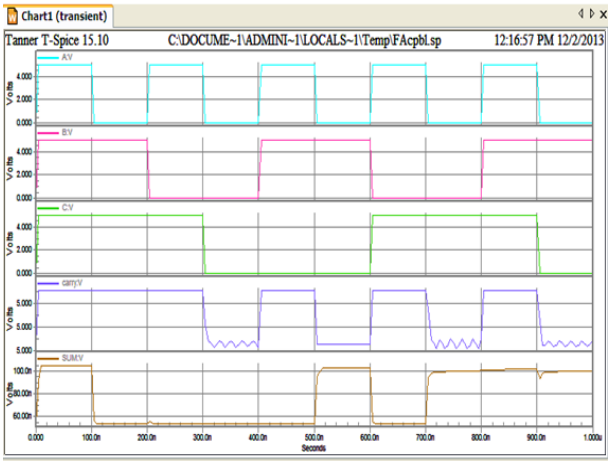

Fig.7Simulation Results of FULL ADDER

DEVICE AND NODE COUNTS

DEVICE	NODE COUNT
MOSFETs	34
MOSFET geometries	2
Voltage sources	8
Sub circuits	7
Model Definitions	5
Computed Models	2
Independent nodes	15
Boundary nodes	9
Total nodes	24

TABLE.1

POWER RESULTS OF FULL ADDER

Voltage Source	Minimum Power	Maximum Power	Average Power in watts
Vvoltage Source_1	0.000000 e^{+000} at time 0	1.120364e^{-003} at time 4.01875e^{-007}	1.784647e^{-006}
VVoltageSource_2	0.000000 e^{+000} at time 0	3.260543e^{-003} at time 5.03568e^{-007}	1.021068e-005
VVoltageSource_3	0.000000 e^{+000} at time 0	1.622141 e^{-004} at time 6.0351e^{-007}	2.363675e^{-007}
VVoltageSource_4	1.89918e-009 at time 4.38529 e-007	2.153464e-002 at time 2.03544e-009	6.957930e-004

B. RIPPLE CARRY ADDER

It is possible to create a logical circuit using multiple full adders to add N-bit numbers. Each full adder inputs a Cin, which is the Cout of the previous adder. This kind of adder is a ripple carry adder, since each carry bit "ripples" to the next full adder. The first full adder may be replaced by a half adder. Here 4-bit ripple carry adder is implemented with the help of four full adder blocks.

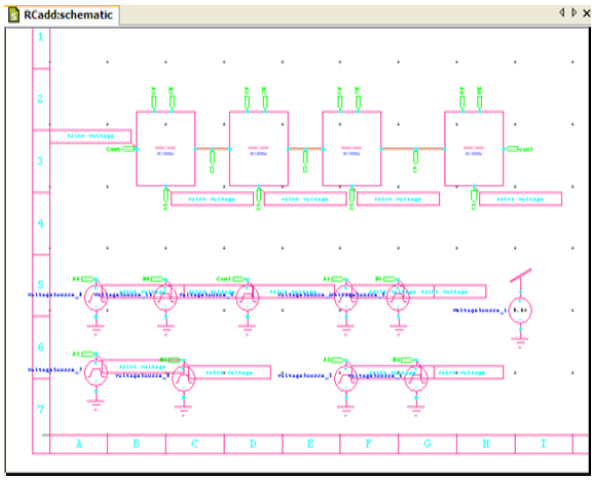

Fig.8 Schematic view of RIPPLE CARRY ADDER

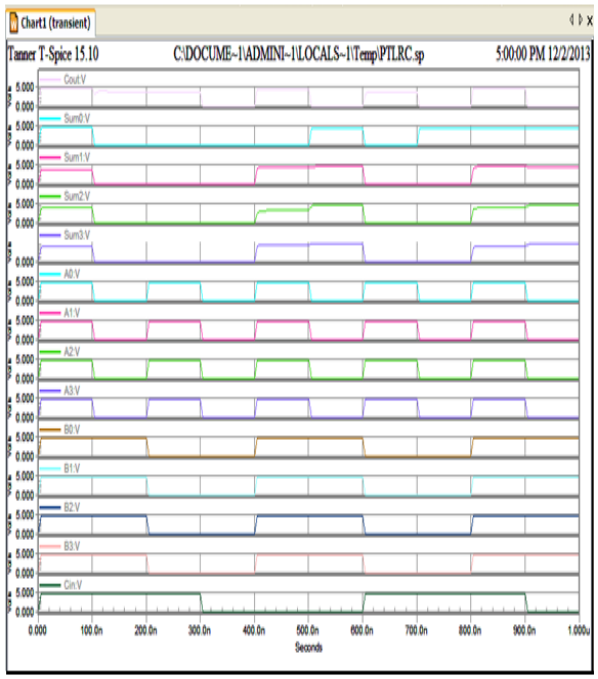

Fig.9 Simulation Results of Ripple Carry Adder

DEVICE AND NODE COUNTS

DEVICE	NODE COUNT
MOSFETs	136
MOSFET geometries	2
Voltage sources	26
Sub circuits	32
Model Definitions	5
Computed Models	2
Independent nodes	60
Boundary nodes	27
Total nodes	87

TABLE.2

POWER RESULTS OF RIPPLE CARRY ADDER

Voltage Source	Minimum Power	Maximum Power	Average Power in watts
VVoltage Source_1	2.18999e-007 at time 4.0552e-007	8.26214e-002 at time 2.0467e-009	1.863877 e-003
VVoltage Source_2	0.000000e+00 at time 0	1.02420e-003 at time 2.11497 e-009	4.514442 e-006
VVoltage Source_3	0.000000e+00 at time 0	4.59133e-003 at time 9.03305 e-007	1.388041 e-005
VVoltage Source_4	0.000000e+00 at time 0	2.40285e-004 at time 1.03234 e-007	3.474678 e-007
VVoltage Source_5	0.000000e+00 at time 0	1.02420e-003 at time 2.11497e-009	4.514442 e-006
VVoltage Source_6	0.000000e+00 0 at time 0	4.59133e-003 at time 9.03305e-007	1.388041 e-005
VVoltage Source_7	0.000000e+00 at time 0	1.02420e-003 at time 2.11497e-009	4.514442 e-006
VVoltage Source_8	0.000000e+00 at time 0	4.59133e-003 at time 9.03305e-007	1.388041 e-005
VVoltage Source_9	0.000000e+00 at time 0	1.120357 e-003 at time 4.01875e-007	1.593048 e-006
VVoltage Source_10	0.000000e+00 at time 0	4.041827e-003 at time 9.03375e-007	1.387071 e-005

C. MULTIPLEXER

A Multiplexer or mux is a combinational circuits that selects several analog or digital input signals and forwards the selected input into a single output line. A multiplexer of 2^n inputs has n selected lines, are used to select which input line to send to the output.

I) 2 to 1 MULTIPLEXER

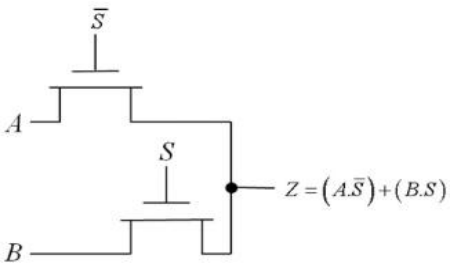

Fig.10 2 to 1 Multiplexer

The pass-transistor logic attempts to reduce the number of transistors to implement a logic by allowing the primary inputs to drive gate terminals as well as source-drain terminals.

II) 4 to 1 MULTIPLEXER

4 to 1 multiplexer is designed by using Three 2 to 1 multiplexers and Two select lines S0 and S1.

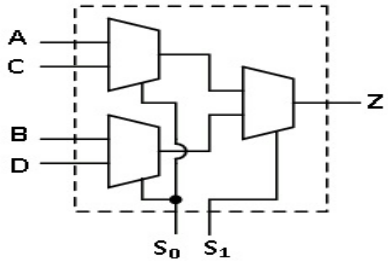

Fig.11 4 to 1 Multiplexer

III) 8 to 1 MULTIPLEXER

8 to 1 multiplexer is designed by using Two 4 to 1 multiplexers, one 2 to 1 multiplexer and Three select lines S0 S1 and S2.

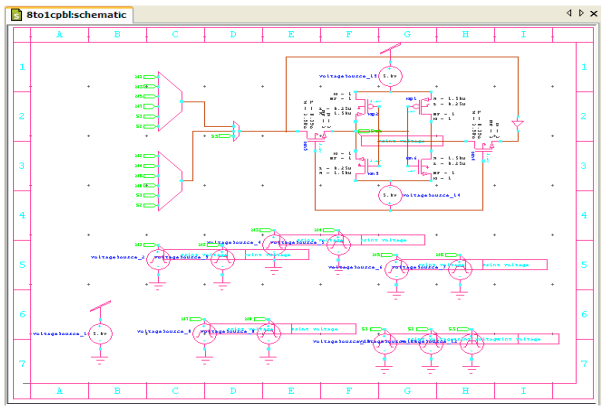

Fig.10 Schematic view of 8 to 1 MULTIPLEXER

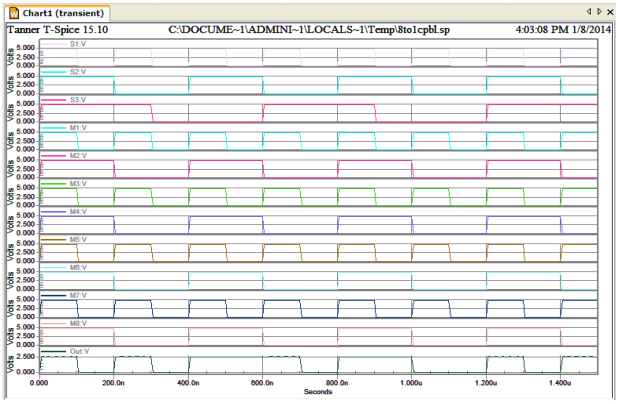

Fig.11 Simulation Results of 8 to 1 MULTIPLEXER

TABLE.3 POWER RESULTS OF 8 to 1 MULTIPLEXER

Voltage Source	Minimum Power	Maximum Power	Average Power in watts
VVoltage Source_1	2.315643e-007 at time 4.0552e-007	2.31564e-002 at time 1.20213e-006	2.160393e-003
VVoltage Source_2	0.000000e+00 at time 0	6.79225e-003 at time 8.05101e-007	1.392748e-003
VVoltage Source_3	0.000000e+00 at time 0	6.79275e-003 at time 4.05101e-007	6.155065e-004
VVoltage Source_4 from time 0 to 1e-006	0.000000e+00 at time 0	6.90510e-003 at time 2.05312e-007	1.539566e-003
VVoltage Source_5	0.000000e+00 at time 0	1.37392e-003 at time 1.00344e-006	2.828287e-006
VVoltage Source_6	0.000000e+00 at time 0	1.63667e-003 at time 2.01841e-007	7.652658e-006
VVoltage Source_7	0.000000e+00 at time 0	6.84930e-003 at time 9.08114e-007	1.298757e-003
VVoltage Source_8	0.000000e+00 at time 0	1.63349e-003 at time 7.03461e-007	5.691632e-006
VVoltage Source_9	0.000000e+00 at time 0	1.49252e-003 at time 4.01605e-007	3.423147e-006
VVoltage Source_10	0.000000e+00 at time 0	3.42314 e-003 at time 4.01605e-007	1.040936e-006
VVoltage Source_11	0.000000e+00 at time 0	1.59591e-004 at time 4.02138e-007	1.815434e-007

VVoltage Source_12	0.000000e+000 at time 0	7.82133e-005 at time 2.19524e-009	1.504963 e-007

IV) ARRAY MULTIPLIER

Array multiplier is an efficient layout of a combinational Multiplier. Multiplication of two binary number can be obtained with one micro-operation by using a combinational circuit that forms the product bit all at once thus making it a fast way of multiplying two numbers since only delay is the time for the signals to propagate through the gates that forms the multiplication array. With its good structure, this multiplier is based on the standard add and shift operations. Each partial product is generated by taking into account the multiplicand and one bit of multiplier each time. The impending addition is carried out by high-speed carry-save algorithm and the final product is obtained employing any fast adder the number of partial products depends upon the number of multiplier bits.

The Schematic of 4x4 Array Multiplier is shown in the following Fig. 12

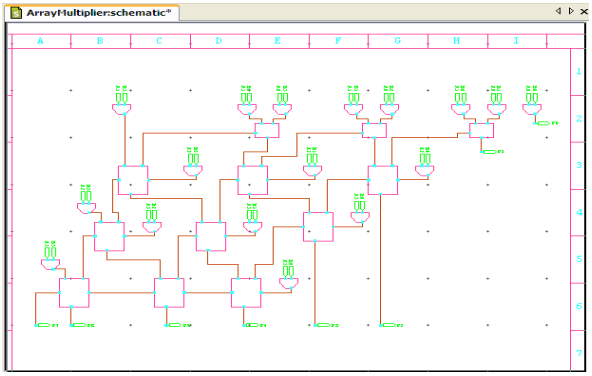

Fig.12 Schematic view of ARRAY MULTIPLIER

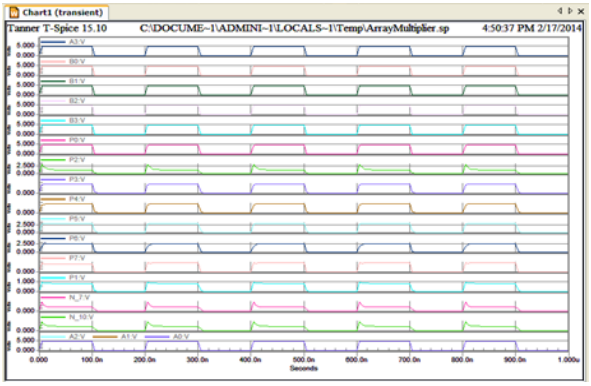

Fig.13 Simulation Results of ARRAY MULTIPLIER

TABLE.4 POWER RESULTS OF ARRAY MULTIPLIER

Voltage Source	Minimum Power	Maximum Power	Average Power in watts
VVoltage Source_1	5.242584e-007 at time 4.03243 e-007	6.918037e-001 at time 3.39658e-009	2.86960 e-001
VVoltage Source_2	0.000000e+00 at time 0	2.43084e-003 at time 1.02125e-007	1.578898 e-006
VVoltage Source_3	0.000000e+00 at time 0	3.04647e-003 at time 1.02088e-007	1.587092 e-006
VVoltage Source_4 from time 0 to 1e-006	0.000000e+00 at time 0	2.37271e-003 at time 3.02142e-007	9.711132 e-007
VVoltage Source_5	0.000000e+00 at time 0	2.86320e-003 at time 1.02125e-007	1.768979 e-006
VVoltage Source_6	0.000000e+000 at time 0	1.27042e-003 at time 2.0571e-007	1.738584 e-004
VVoltage Source_7	0.000000e+00 at time 0	1.18083e-003 at time 2.05e-007	1.398516 e-004
VVoltage Source_8	0.000000e+00 at time 0	8.76650e-004 at time 8.04358e-007	5.968264 e-006
VVoltage Source_9	0.000000e+00 at time 0	1.66791e-003 at time 4.6004e-009	2.139657 e-005

VI.. CONCLUSION

Adiabatic circuits offers reduction in the power dissipation for the VLSI circuits. Adiabatic circuits adopt a gradually rising and falling power-clock, can result in a considerable energy saving. NMOS Full Adder, Ripple Carry Adder, 8 to 1 Multiplexer and Array Multiplier are proposed using CPBL techniques. CPBL consist of two parts: the Complementary Pass Transistor network and 4-tr Boost Stage, fulfilling the logical evaluation and signal amplification respectively. It is fully powered by 2-phase alternating sinusoidal power clocks Pc and ~Pc produced by RLC resonant circuit. To demonstrate the performance and energy efficiency, 4-Ripple Carry Adder is implemented by CPBL, CPAL which is similar structure. The CPBL implementation reduces about 65% energy compared with the static CMOS and dissipates less energy with respect to CPAL.

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