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Photovoltaic Grid-Connected System Based On Cascaded Quasi-Z-Source Network

T. Hari Hara Kumar[1], P. Aravind[2]

Final Year B.Tech, Dept. of EEE, K L University, Guntur, AP, India[1]

Final Year B.Tech, Dept. of EEE, K L University, Guntur, AP, India [2]

ABSTRACT: Renewable energy sources are being widely used for Distributed Generation (fuel cells, solar panels, Wind power generators etc..,) because of their advantages. But they produce a very low output voltage. To interconnect a low-dc-voltage to residential loads a special voltage matching converter is required. This paper presents a back to back connection of cascaded quasi-Z-source network based step up DC/DC converter and 3-level diode clamped inverter. The proposed system reduces the component stresses and size of the converter. This network provides voltage boost and buck functions in single stage without any additional switches by the introduction of special switching strategy. The proposed cascaded qZSI inherits all the advantages of the traditional solution (voltage boost and buck functions in a single stage, continuous input current, and improved reliability). The results are analyzed by Matlab-Simulink environment.

KEYWORDS: Distributed Generation, Quasi Z Source network, Clamped, Shoot through and Non-Shoot through states.

I.INTRODUCTION

More efforts are now being put into distributed power generation of renewable energy sources (RESs), such as photovoltaic (PV), wind power, and fuel cells, which are sustainable and environmental friendly. Practically, several distributed generations (DGs) consist of distributed power grid and further construct microgrid with local loads and managements. To ensure proper performance of the microgrid, DG is usually required to work in two modes: stand alone and grid connected. As an interface between RES and distributed power grid, the selection of power electronic converter becomes a hectic task.

There exist two traditional inverters: voltage-source (VSI) and current-source (CSI) inverters. In VSI, a constant voltage source acts as input to the inverter bridge. The constant voltage source is obtained by connecting a large capacitor across the DC source. In CSI, a constant current source acts as input to the inverter bridge. The constant current source is obtained by connecting a large inductor in series with the DC source. Typical inverters (VSI and CSI) have few disadvantages. They are listed below:

1. Behaves as either boost or buck operation only. Thus the obtainable output voltage range is limited, either smaller or greater than the input voltage.
2. Vulnerable to EMI noise and the devices gets damaged in either open or short circuit conditions.
3. The combined system of DC-DC boost converter and the inverter has lower reliability.

To overcome these disadvantages a new concept was developed in year 2002 by Dr. F.Z. Peng. This involves combination of VSI and CSI to form a cross coupled network of two inductors and two capacitors, known as Impedance Network. Z-source inverter (ZSI) is known as a single-stage buck/boost inverter. With an impedance network coupling the inverter main circuit to the DC source, the ZSI achieves voltage buck/boost in one stage, without introducing more switching devices. Shoot-through state enables energy to be stored in inductors, which is released when at non-shoot through state, followed by the voltage boost feature. For the voltage-fed type ZSI (abbreviated as ZSI), voltage boost methods based on pulse width modulation (PWM) have been first investigated as simple boost control, maximum boost control, and maximum constant boost control. With a set of new topologies of the impedance networks, a class of quasi-Z-source inverter (qZSI) has been derived from the original ZSI and applied to DG applications. A voltage-fed qZSI (shown in Fig. 1(a)) was proposed for PV applications because of continuous input

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current and reduced passive component (capacitor) rating—capacitor voltage on C_2 is much less than that on C_1 during operating and this feature leads to lower manufacture cost. This paper discusses a method of performance improvement for the voltage-fed qZSI with continuous input current gained by the introduction of the cascaded quasi-Z-source network (qZS-network). The cascaded (two-stage) qZS-network is derived by the adding of one diode (*D*2), one inductor (*L*3), and two capacitors (*C*3 and *C*4) to the traditional qZSI, as shown in Fig. 1(b). This paper further proposes a new grid connected system which comprises of front end high step up conversion and 3-level level inverter. Front end high step up conversion comprises of a cascaded qZI, a high frequency isolation transformer and a voltage doubler rectifier (VDR)

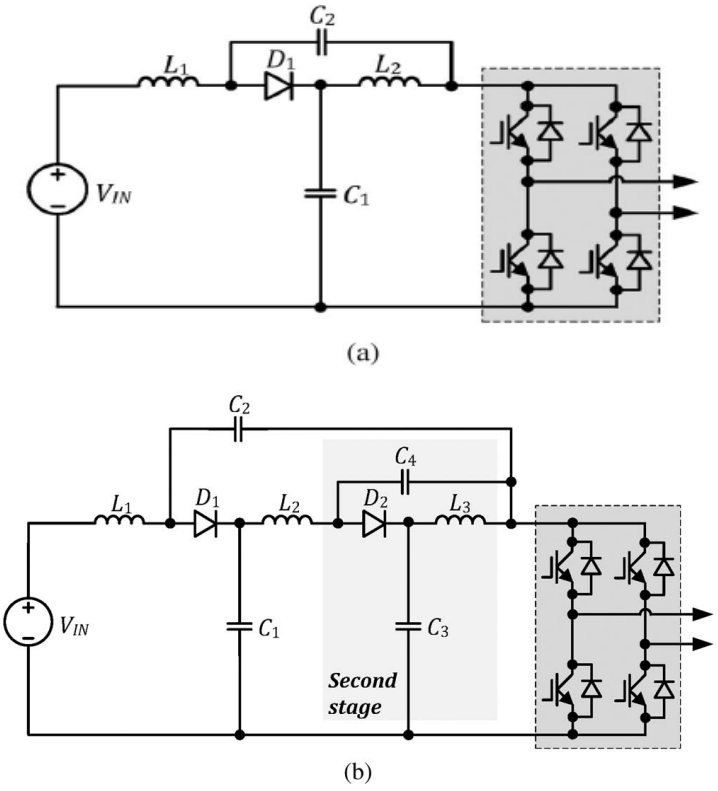

Fig. 1 a) qZSI b) Cascaded qZSI

II.PROPOSED BLOCK DIAGRAM

The main focus of this paper is on the power converter (PC) for residential power systems. PCs are used to interconnect distributed energy sources producing low dc voltage, like solar panels (typically 40–80 V dc), to the residential loads (typically 3 × 400 V_{ac}). Due to safety and dynamic performance requirements, the PC should be realized within the dc/dc/ac concept. This means that low voltage from the energy source first passes through the front-end step-up dc/dc converter with galvanic isolation afterwards, the output dc voltage is inverted with the three-phase inverter and filtered to comply with the imposed standards and requirements (second dc/ac stage). Our novel approach to the front-end step-up dc/dc converters provides a very high voltage gain. The block diagram of proposed grid connected system is shown in figure 2.

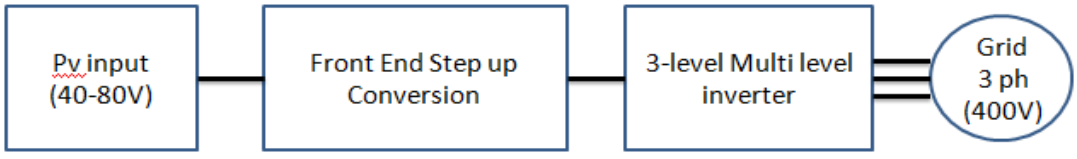

Fig. 2 Proposed Block Diagram

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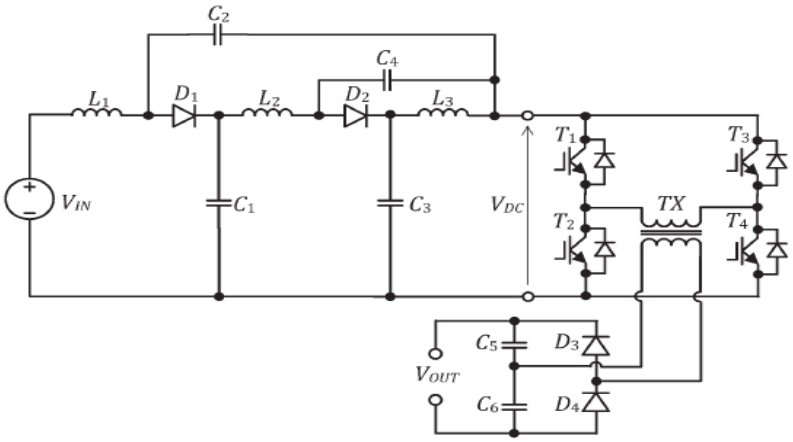

Fig. 3 Front end high step up conversion

The front end high step up conversion is shown in fig 3.The most important stage in step up conversion is cascaded qZSI. The equivalent circuits of cascaded qZSI in respective active and shoot through states are shown in fig 4. As the input voltage of PV varies, to regulate the varying input voltage, the front-end qZSI has two different operating modes: shoot-through and non-shoot through. In the non-shoot-through mode, the qZSI performs only the voltage buck function. This operation mode is typically used during light-load conditions, when the output voltage of a solar panel reaches its maximum. The inverter is controlled in the same manner as with the traditional VSI, utilizing only the active states when one and only one switch in each phase leg conducts. When the input voltage drops below some predefined value, the qZSI starts to operate in the shoot through mode. In order to boost the input voltage during this mode, a special switching state (the shoot-through state) is implemented in the pulse width modulation (PWM) inverter control.

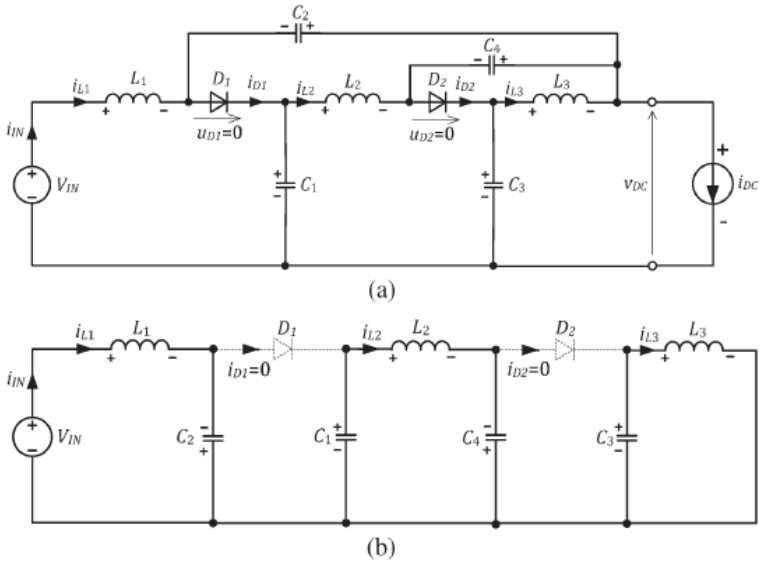

Fig. 4 Equivalent circuits of the cascaded qZS-network:
(a) During the non shoot through (active) state and (b) during the shoot-through state.

The PWM switching states sequence presented in Table 1 shows that the upper and lower switches operate with different switching frequencies. The switching frequency of the upper switches (*T1* and *T3*) in the shoot-through mode is equal to the fundamental frequency of the isolation transformer, while the switching frequency of the lower switches (*T2* and *T4*) is three times higher than that of *T1* and *T3*.

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State	T1	T2	T3	T4
Zero state	1	0	1	0
Shoot-through	1	1	1	1
Zero state	1	0	1	0
Active state 1	1	0	0	1
Zero state	1	0	1	0
Shoot-through	1	1	1	1
Zero state	0	1	1	0
Active state 2	0	1	1	0

Table 1: PWM switching states of qZSI

The operating period of the PWM inverter during the shoot-through mode consists of an active state t_A, a zero state t_Z and a shoot-through state t_S:

$$T = t_A + t_Z + t_S$$

The above equation could also be represented as:

$$\frac{t_A}{T} + \frac{t_Z}{T} + \frac{t_S}{T} = D_A + D_Z + D_S = 1$$

Where, D_A - duty cycle of the active state
D_z - duty cycle of the zero state
D_S - duty cycles of the shoot-through state.

Operation of voltage-doubler rectifier:
To reduce the turns ratio of the isolation transformer the voltage doubler rectifier (VDR) is implemented on the secondary side of the converter. In contrast to the traditional full-bridge rectifier, two diodes of one leg in the VDR topology are replaced by the capacitors. The operation principle of the VDR is explained in Fig. 5.

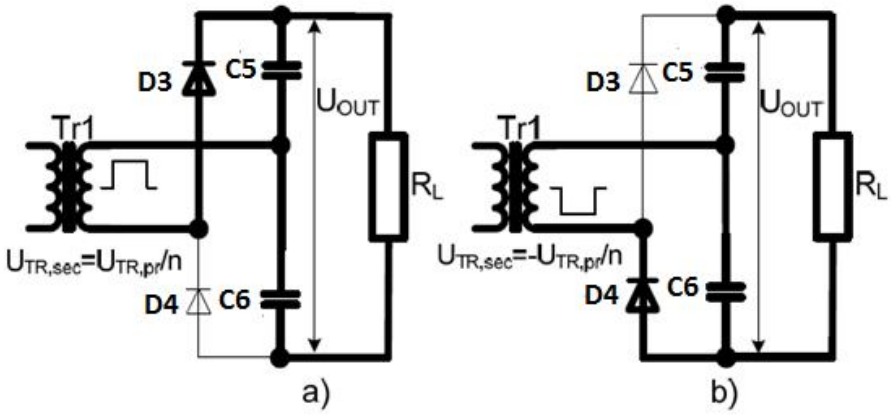

Fig. 5 Operation principle of VDR

During the positive half cycle, the capacitor *C5* is charged through the diode *D3* to the peak secondary voltage of the isolation transformer. During the negative half cycle the capacitor *C6* is charged through diode *D4*. At every time instant the output voltage from this circuit will be the sum of the two capacitor voltages or twice the peak voltage of the secondary winding of the isolation transformer.

Therefore, $U_{out} = 2*U_{TR,sec}$

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III. 3-LEVEL MULTI LEVEL INVERTER

Conventional 2-level PWM inverters generate high dv/dt and high frequency common mode voltages which deteriorate the performance of electrical appliances. Due to capacitor voltage unbalancing, neutral point potential also varies from zero. Recently, multilevel inverters have been found wide acceptability in medium and high voltage applications. Multilevel inverters have the advantage of producing high voltage-high power with improved power quality of the supply. It also eliminates the use of problematic series-parallel connections of switching devices. However, multilevel PWM inverters generate common mode voltages as in the case of conventional 2-level inverters.

Fig. 6 shows the very popular topological structure of diode clamped 3-phase, 3-level inverter. The switching states of the inverter are shown in Table 2 for one leg. It gives the output pole voltage V_{AO}, output line voltage V_{AB} and switch state. Switch state '1' means 'on' and '0' means 'off'. This switching pattern can be achieved by means of different multilevel control strategies such as square wave switching, sine-triangle comparison method (SPWM), space vector modulation (SVM), selective harmonic elimination technique, hysteresis current control, sigma-delta modulation etc. Of these methods, sinusoidal pulse width modulation (SPWM) is the simple and cost effective method to implement.

The major advantages of the diode clamped inverter can be summarized as follows:

1. When the number of levels is high enough, the harmonic content is significantly low to avoid the need of filters.
2. Inverter efficiency is high because all devices are switched at the fundamental frequency.
3. The control method is simple.

The major disadvantage of the diode clamped inverter can be summarized as follows:

1. Excessive clamping diodes are required when the number of levels is high.

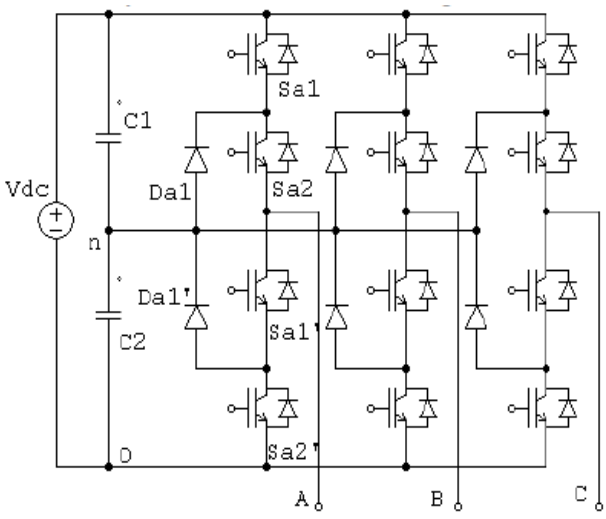

Fig. 6 diode clamped 3-phase, 3-level inverter

V_{AB}	Output Pole Voltage (V_{AO})	Switch States			
		S_{a1}	S_{a2}	S_{a1}	S_{a2}
$-V_{dc}/2$	0	0	0	1	1
0	$V_{dc}/2$	0	1	1	0
$V_{dc}/2$	V_{dc}	1	1	0	0

Table 2: Switching states for one leg

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IV.RESULT AND DISCUSSION

The MATLAB-SIMULINK model of the qZSI-based DC/DC converter was developed and simulations made to analyze the proposed system. For all simulations the input voltage of the converter was set to 40-80V and the values of inductances in qZSI are 100µH and capacitances are 370µF. The turn's ratio of isolation transformer is 1:3.75 with frequency 5 kHz. Capacitance values in VDR are 720µf. The input voltage, primary winding and secondary winding waveforms of isolation transformer and voltage profiles of the capacitors in qZS-network were measured. The whole model of step up conversion is shown in Fig 7.

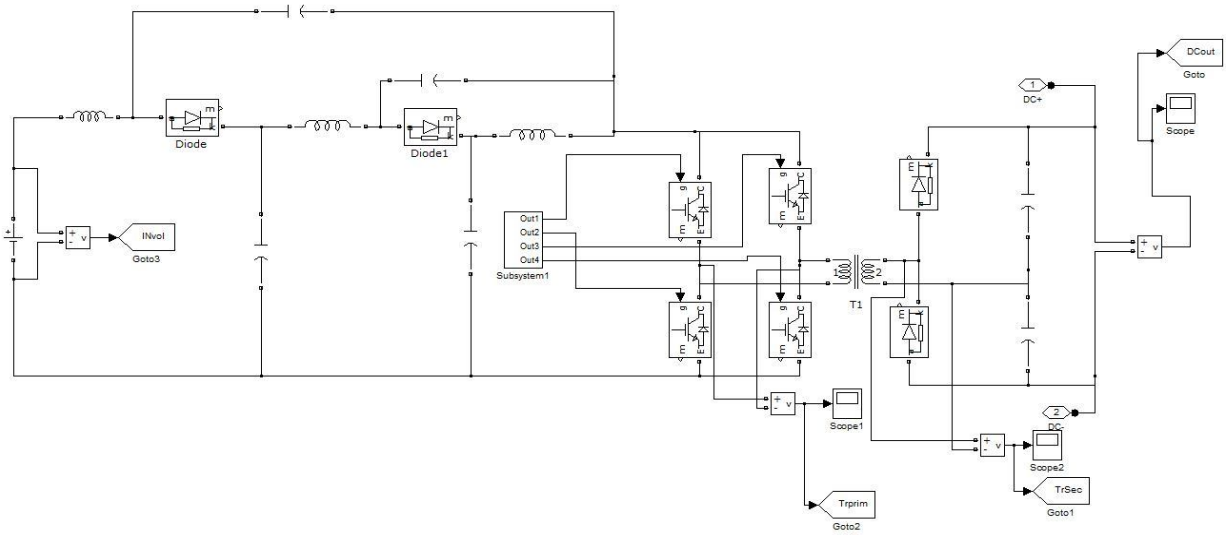

Fig. 7 Simulink diagram of front end step up conversion

The outputs measured from the power converter are shown in figure 8. Isolation transformer primary winding voltage is 80V and secondary winding voltage is 300V and the total voltage obtained from the VDR is 600V (i.e.., double of the secondary winding voltage)

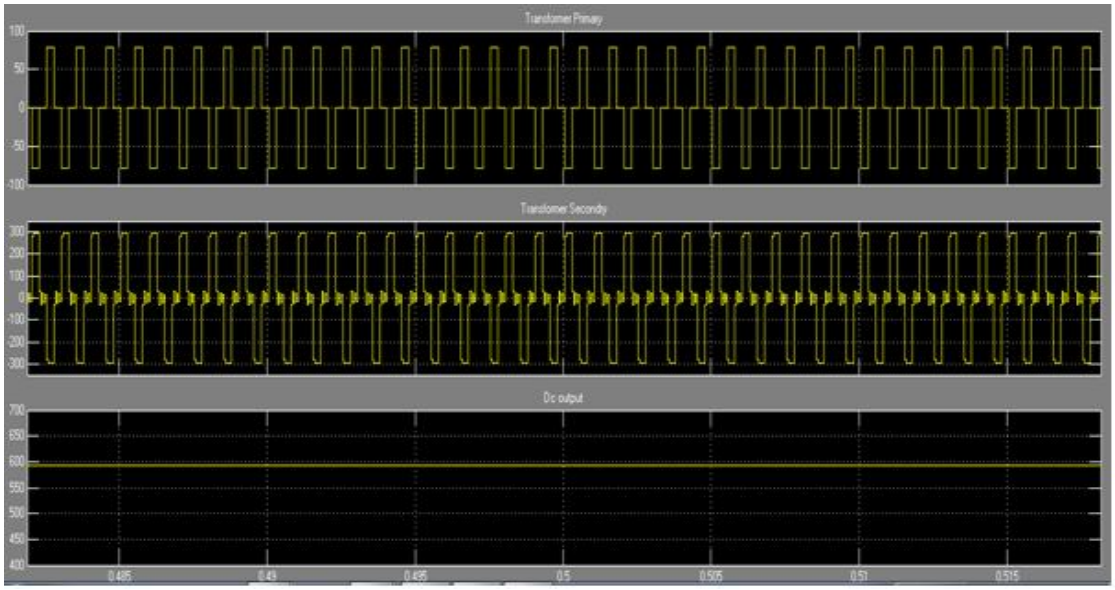

Fig. 8 (a) Transformer primary voltage
(b) Transformer secondary voltage (c) Total output Voltage

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The whole model of diode clamped 3-level inverter is shown in figure 9. The output (600V) of voltage doubler rectifier is given to the inverter to produce ac output voltage of 3 × 400 V_{ac}.

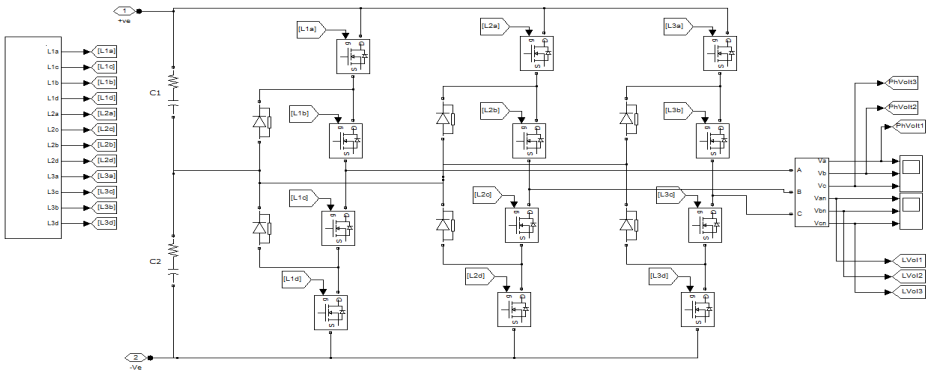

Fig. 9: Simulink diagram of 3ph 3 level diode clamed inverter

One of the most straightforward methods of describing SPWM is to illustrate the intersection of a modulating signal (duty cycle) with triangle waveforms. Figure 10 demonstrates the sine-triangle method for a three-level inverter. The *a* , b ,c phase duty cycle is compared with two (*n*-1 in general) triangle waveforms. Where n is the level of the inverter.

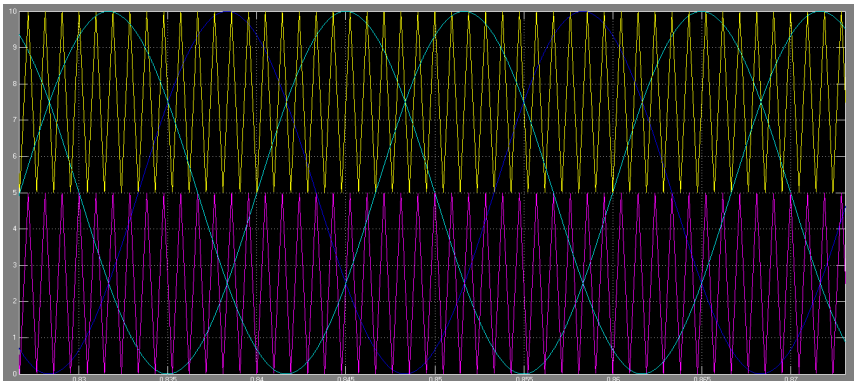

Fig. 10 Sine-Triangular Comparison of 3 level diode clamped inverter

Output line voltage waveform of the inverter is shown in figure 11. Generally an n-level inverter has n levels in phase voltage and 2n-1 levels in line voltage. So for 3-level inverter there will be 5-levels in line voltage as shown.

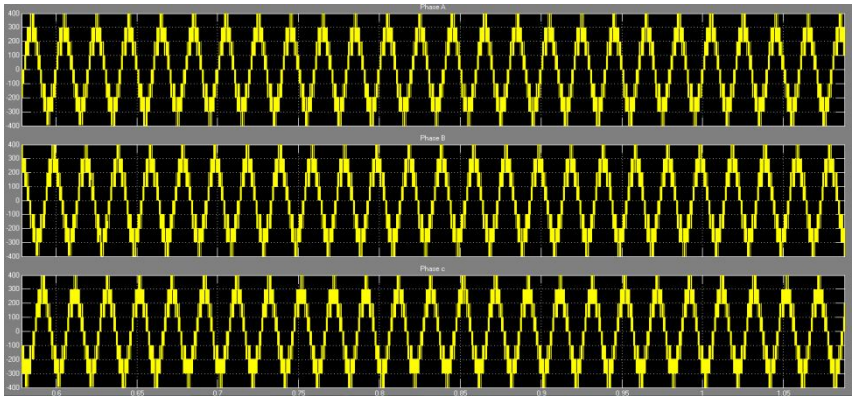

Fig. 11 Inverter output voltage wave forms without filters

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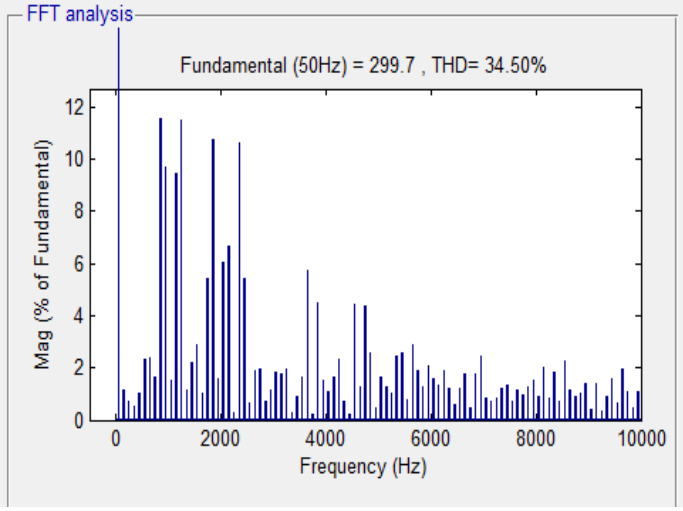

Fig. 12 FFT analysis of inverter output voltage without filters

The figure 12 shows the harmonic spectrum of inverter output voltage. By using the multi level inverters we can reduce the usage of bulky filters. By using more levels harmonics can be reduced drastically. Table 3 shows the voltages at different levels of the system.

PV input	40-80V
Transformer Primary	80V
Transformer Secondary	300V
VDR output	600V
Inverter output line voltage	400V (grid voltage)

Table3: Voltages at different levels

The results demonstrate that the proposed converter operates correctly, thus ensuring a ripple-free intermediate dc voltage V_{OUT}. Also it is confirmed that the proposed converter ensures stable 3 × 400 Vac_{rms} 50-Hz output voltage within the predefined input voltage.

V.CONCLUSION

This paper overcomes the problem with voltage source inverter by using Quasi Z Source network. To decrease the shoot through duty cycle at same voltage boost factor cascaded connection of qZSI is used and for further decreasing the shoot-through duty cycle the number of stages of the qZS-network could be increased. The usage of voltage doubler rectifier (VDR) results in less turns of ratio in isolation transformer. To decrease the stresses on the switches the PWM inverter is replaced by diode clamped multi level inverter. From results it is proven that the proposed front end high step up conversion has ripple free intermediate dc voltage and it is also confirmed that the proposed converter ensures stable 3 × 400 Vac_{rms} 50-Hz output voltage within the predefined input voltage.

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BIOGRAPHY

Tummala Hari Hara Kumar is currently pursuing his B.Tech Degree in K L University, Vaddeswaram, Guntur District, Andhra Pradesh, India. He is currently the student Technical Head of KLU-IEEE Student Branch. His Research interest includes Power Electronics, Power Systems, Control Systems and Grid-Connected Systems.

Aravind Piratla Is Currently Pursuing His B.Tech Degree In K L University, Vaddeswaram, Guntur District, Andhra Pradesh. He Is Currently The Student Chair Of KLU-IEEE Student Branch. His Research Includes Power Electronic, Power Systems And Plug-In Electric Vehicle's.