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Power Optimization in FPGA through Controller Device

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ABSTRACT: Field programmable Gate Arrays (FPGAs) are widely used for implementation of digital system design due to their flexibility, low time-to-market, growing density and speed. But the power consumption, especially leakage and dynamic power has become a major concern for semiconductor industries. FPGAs are less power efficient than custom ASICs, due to the overhead required providing programmability. Despite this, power has been largely ignored by the FPGA research community earlier, whose prime focuses on power too. Hence this paper demonstrates some of the most utilized and efficient techniques for power optimization and reduction in FPGAs currently. The Clock gating methodology based on voltage scaling is proposed in this paper. Dual Supply voltage design is widely accepted as an effective way to reduce the power consumption of CMOS circuit. The Coarse Grained Clock network technique is utilized to minimize clock network power in FPGA device.

KEYWORDS FPGA, Power Reduction, clock skew, dual Vdd.

I. INTRODUCTION

Field-Programmable Gate Arrays (FPGAs) are integrated circuits that can be programmed to implement any digital circuit. The main difference between FPGAs and conventional fixed logic implementations, such as Application Specific Integrated Circuits (ASICs), is that the designer/customer programs the FPGA on-site[1-3].For fixed logic, the designer must create a layout mask and send it to a foundry to be fabricated. Creating a layout is labor-intensive and requires expensive CAD tools and experienced engineers. Programmable switches controlled by configuration memory occupy a large area in the FPGA and add a significant amount of parasitic capacitance and resistance to the logic and routing resources.

Many studies have focused on reducing the speed and area overhead of FPGAs. Important advancements include cluster-based logic blocks[4], which improve speed by grouping the basic logic elements of the FPGA into clusters with faster local interconnect; embedded memories[5], which reduce the speed and area overhead for applications with storage requirements; and embedded ALUs[6], which reduce at the speed and area overhead for applications that perform arithmetic operations. As CMOS process technology scales down, the power density continues to increase due to higher chip operating frequencies, higher total interconnect capacitance per chip, and increasing leakage. Indeed, the International Technology Roadmap for semiconductors has identified low-power design techniques as a critical technology need[7].

POWER CONSUMPTION

Due to the dramatic increase in portable and battery-operated applications, lower power consumption has become a necessity in order to prolong battery life. Power consumption is an important part of the equation determining the end product's size, weight, and efficiency. FPGAs are becoming more attractive for these applications due to their shorter product life cycle. FPGAs are programmable, so they allow product differentiation. Selecting an appropriate FPGA architecture is critical in achieving the best static and dynamic power consumption. As per we are dealing with Power optimization & reduction techniques. The two components to power consumption: static, dynamic.

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Dynamic power is the power dissipated during active state due to switching activity of input signal [5].In other words, dynamic power dissipation is caused by the charging. Since an input can change without necessarily resulting in logic transition in the output, dynamic power can be dissipated even when an output does not change its logic state. The dynamic power dissipation is the result of charging and discharging parasitic capacitances. Dynamic power dissipation in a circuit is given as,

$$P_{dynamic}=\sum(\alpha\ f_{clk}\ C_L\ V^2_{dd})$$

Where C is the load capacitance, V_{dd} is the operating voltage,α is the activity factor of that net (the probability that net will switch in a given cycle) and f is the operating frequency of the node. The techniques to reduce Dynamic Power consumption are, Clock Gating, Power Gating, Improved switching activity, Glitch removal, Pipelining, Guarded Evaluation.

II. LITERATURE SURVEY:

In previous work single voltage is applied to the whole circuit. The power consumed is high as both active and inactive blocks use the same supply voltage. This power consumption degrades the system performance and life time of portable application. In order to overcome this drawback, we propose dual Vdd technique along with controller device. As the switching power is quadratically related to the supply voltage, the power consumption is effectively reduced.

Power gating techniques can be classified into two types: coarse-grain power gating and fine-grain power gating. Low power FPGA architecture is generated with the use of fine grained Vdd control scheme called micro Vdd-hoping[8].The Vdd of each block is varied between the higher V_{DD} and lower V_{DD} spatially and temporalily to achieve low power. In fine grained power gating technique each lookup table have its own controller device. So the number of controllers used in fine grained technique is much larger than that of coarse grained technique. In this technique the controller device is always running. This results in large area and dynamic power overheads. Due to these overheads fine grained technique is less efficient than the coarse grained technique.[9]

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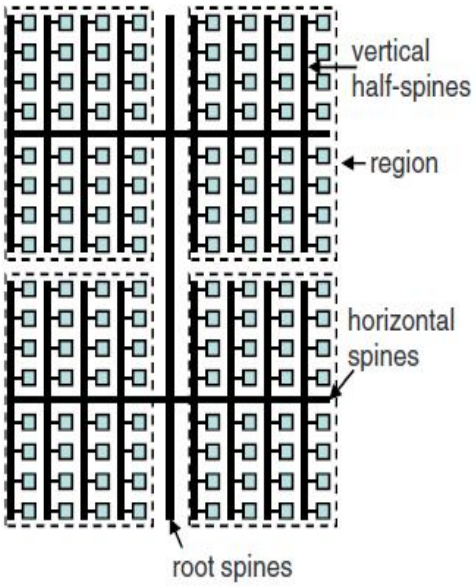

Figure 2.1 Coarse grained Architecture

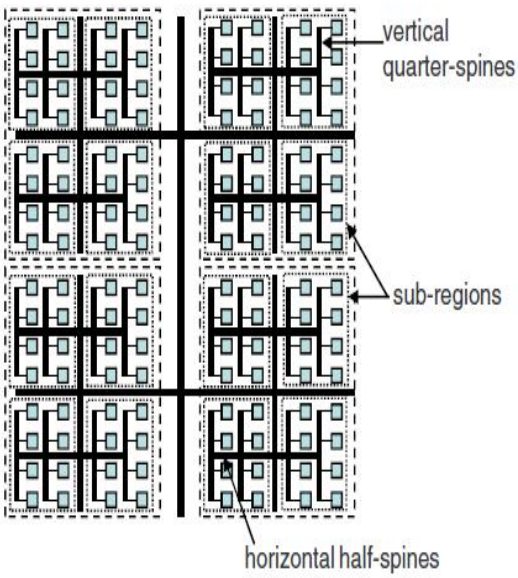

Figure 2.2 Fine grained Architecture

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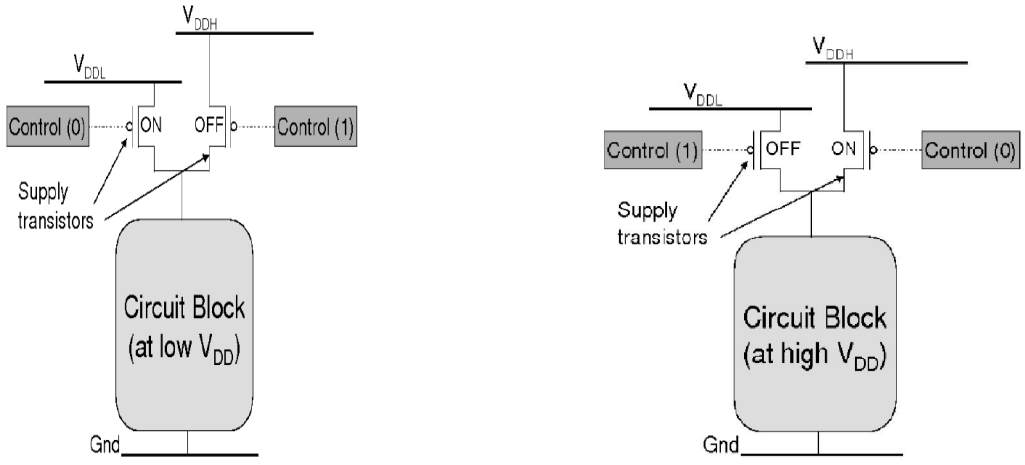
In coarse-grain power gating, a large number of LUTs share a single sleep controller so the area and power overheads of the sleep controller are relatively small.

III. PROPOSED METHOD:

Reducing the supply voltage (V_{DD}) is an effective technique for reducing both dynamic and static power. Dynamic power has a quadratic dependency on supply voltage, while both sub-threshold leakage and gate leakage exhibit exponential dependencies on the supply voltage. However, reducing supply voltage also negatively affects circuit performance. A well-known technique to reap the benefits of voltage scaling without the performance penalty is the use of dual-V_{DD}. The active blocks in the design operate on the normal V_{DD} (or V_{DDH}), while inactive blocks operate on a second supply rail with a lower voltage (or V_{DDL}). While dual- V_{DD} ICs have been successfully used in low-power ASICs and custom ICs [12], no commercial FPGA today uses multiple V_{DD} for power reduction.The difficulty of designing a dual-V_{DD} FPGA is that the optimal V_{DD} assignment changes from one design to another.

Consequently, if logic blocks are statically determined to be operating at low or high V_{DD}, the placement and routing algorithms need to be modified accordingly as in [11]. However, static assignment of V_{DD} to the blocks may prevent the ability to reduce power consumption or to meet timing constraints for some designs. In contrast, the use of V_{DD}-programmability for each block helps to tune the number of high and low V_{DD} blocks as desired by the application. In this approach, the challenge is in determining the V_{DD} assignments to each block. Furthermore, positioning of the controller influences the ability to assign lower V_{DD} to the routing blocks. In our programmable dual-V_{DD} architecture (figure 3.1), the V_{DD} of a circuit block is selected between V_{DDH} and V_{DDL} by using two high-VT transistors (supply transistors) connecting the block to the supplies. The state (ON/OFF) of each supply transistor is controlled by a configuration bit.



(a) (b)

Figure 3.1 Supply Transistors used for programmable V_{DD}

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IV. SIMULATION RESULTS

Comparison is made for various supply voltage scaling and it is found that power consumed by our Dual V_{DD} technique is lesser than without controller device and also I_{dd} is analyzed in Table4.1.

Table 4.1Comparison of Power Dissipation without Controller and with Controller

WITHOUT CONTROLLER			WITH CONTROLLER		
$_{Voltage}$(V)	Power(mW)	I_{dd}(mA)	Voltage(V) V_{DDH} V_{DDL}	Power(µW)	I_{dd}(mA)
1	0.107	1.186	1 0.8	48.153	1.205
3.3	0.143	1.169	3.3 1.2	85.326	1.186

V. CONCLUSION

We have presented a dual-V_{DD} FPGA architecture that provides significant power savings with minimal performance penalty. Variations of the V_{DD} assignment and controller device were explored. The dynamic power was reduced around 45- 60%. Power supply network to support dual V_{DD} or configurable V_{DD} may introduce extra routing congestion. The total power reduction percentage for dual V_{DD} FPGAs is significantly lower than the logic power reduction percentage. we will study how to reduce interconnect power by dual V_{DD} in future

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