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Power Saving for Merging Flip Flop Using Data Driven Clock Gating

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ABSTRACT: Data-driven clock gating is reducing the total power consumption of VLSI chips. There, flip-flops are merged and share a common clock signal. Finding the optimal clusters is the key for maximizing the power savings. To reduce the hardware overhead involved, flip-flops (FFs) are merged so that they share a common clock enabling signal. Power optimization system to decrease clock power by using Multibit flips flop. Clock gating one can save power by reducing redundant clock activities confidential the clock modules. In this technique to reduce power saving by merging flip flops and integrated clock gating circuit (ICG). Our data-driven clock gating is unified into an Electronic Design Automation (EDA) profitable backend design flow, succeeding total power reduction for various types of important modern industrial and academic designs in 40 and 65 nanometer process technologies. These savings are achieved on top of the savings obtained by clock gating synthesis performed by profitable EDA tools, and gating physically inserted into the register transfer level design.

KEYWORDS: Multibit flips Flop, Integrated Clock Gating Circuit, Optimal Clusters, Data-Driven Clock Gating.

I.INTRODUCTION

The introduction of integrated circuits (ICs), commonly referred to as microchips or simply chips, was accompanied by the need to test these devices. Small-scale integration (SSI) devices, with tens of transistors in the early 1960s, and medium scale integration (MSI) devices, with hundreds of transistors in the late 1960s, were relatively simple to test. However, in the 1970s, large-scale integration (LSI) devices, with thousands and tens of thousands of transistors, created a number of challenges when testing these devices. In the early 1980s, very-large-scale integration (VLSI) devices with hundreds of thousands of transistors were introduced. Steady advances in VLSI technology have resulted in devices with hundreds of millions of transistors.

One of the major dynamic power reduced by clock gating method in computing and consumer electronics products in the overall system's clock signal then reduce the 30%–70% of the total dynamic power consumption [2] and then reduce the overall circuit power to reduce15- 20% of Grouping Flip Flop data driven clock gating method [1].Clock gating is major method of educing clock signal. Generally, when a logic unit is clocked, it is based on the sequential elements receiving the clock signal, sequentially they will toggle in the next cycle whether it is required or not. The data driven clock gating circuit using clock enabling signals are manually added for every FF as a part of a design methodology [1].

With clock gating, the clock signals are ANDed with explicitly predefined enabling signals. Clock gating is employed at all levels of system architecture, block design, logic design, and gates. Several methods to take advantage of this technique are described, with all of them depending on various heuristics in an attempt to increase clock gating opportunities[7]. With the rapid increase in design complexity, computer aided design tools supporting system-level hardware description have become commonly used. Although substantially increasing design productivity, such tools require the employment of a long chain of automatic synthesis algorithms, from register transfer level (RTL) down to gate level and net list [8]. Unfortunately, such automation leads to a large number of unnecessary clock toggling, thus

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increasing the number of wasted clock pulses at flip-flops (FFs) as shown in this paper through several industrial examples.

In this paper, a model for data-driven gating is developed based on the toggling activity of the constituent FFs. The optimal fanout of a clock gater yielding maximal power savings is derived based on the average toggling statistics of the merging FFs, process technology, and cell library in use [10]. In general, the state transitions of FFs in digital systems depend on the data they process. Assessing the effectiveness of data-driven clock gating requires, therefore, extensive simulations and statistical analysis of the FFs activity. Another grouping of FFs for clock switching power reduction, called Multibit FF (MBFF). MBFF attempts to physically merge FFs into a single cell such that the inverters driving the clock pulse into its master and slave latches are shared among all FFs [5]. MBFFs the advantages are: 1) smaller design area due to shared clock drivers and less routing resource 2) Less delay and less power of clock network due to fewer clock sinks 3) Controllable clock skew because of common clock and enable signals for the group of flip-flops and reduced depth of a clock tree [4].

II. DATA DRIVEN CLOCK GATING

A data-driven clock gating circuit is shown in Fig. 1. By XORing gate its output with the present input of Integrated Clock Circuit that will appear at its output in the next clock cycle, an FF checks whether its state is subject to change, thus finding out whether its clock can be disabled in the next cycle. The outputs of k XOR gates are ORed and then latched to generate a joint gating signal for k FFs. The combination of a latch With AND gate is called Integrated Clock Gate (ICG), commonly used by industrial electronic design automation (EDA) tools.

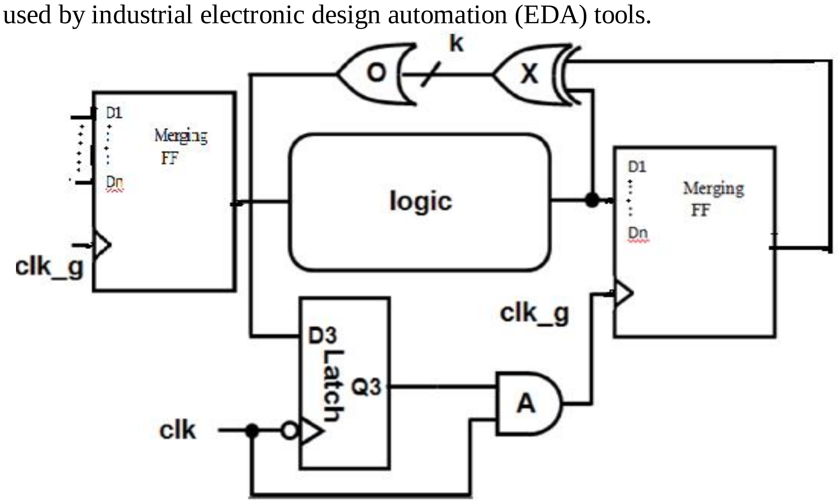

Fig. 1 Circuit diagram of practical Data Driven Clock Gating

The practical Data Driven Clock Gating block diagram is given above. The function of module list is given that State Change Detector, Multi-Bit Flip-Flops and Integrated Clock Gating.

a. Clock Gating

Clock gating circuit is power consumed by 50 % of dynamic power. The clock gating reduce dynamic power by combinational logic circuit and then the circuit reduce clock pulse and sharing the clock signal in merging flip-flops and reduce clock signal. The profitable EDA tools are supported clock gating technique. There are two types of clock gating technique. They are Latch-based clock gating and Latch-free clock gating. The latch-free clock gating technique uses a simple AND or OR . The latch-based clock gating technique is a level-sensitive. In this project using in latch-based clock gating technique. The latch-based clock gating technique is called Integrated Clock Gate (ICG). The Integrated Clock clock will be disables in the next cycle by XORing the output of the present data input and it will reveal at the output in the next cycle. Then the output of the XOR gates are ORed for generating the gate signal for the FF's which is to be used to avoid the glitches. The Integrated clock gate (ICG) can be used by the environmental tools

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by the combination of LATCH with the AND gate. These latches could be used in ultra-low power applications for a digital filter. The data driven clock gating signal are being used as an enabling signals in this applications. There will be a trade-off for ICG is the number of clock pulses could be disabled. The pulses could also be a trade-off for the hardware over-head. While increase the number of flip-flops the hardware overhead decreases to obtain by ORing the enable signals. The level of this high and the low state of signals could be processed in the same versa to give the proper output.

b. Multi-Bit Flip-Flops

Multi-Bit Flip-Flops is an effective method to reduce clock power consumption. Multi-Bit Flip-Flops can significantly reduce the number of individual loads on the clock tree, reducing overall dynamic power used in the clock tree. Area and leakage power saving can also be achieved simply by sharing the clock inverters in the flip flops with a single structure. Multi-Bit Flip-Flops provide a set of additional flops that have been optimized for power and area with a minor trade-off in performance and placement flexibility. The Flip flops share a common clock pin, which decrease the overall clock loading of the N Flops in the Multi-Bit Flip-Flops cell, reduces area with a corresponding reduction in leakage and reduce dynamic power on the clock tree significantly.

c. State Change detector

State Change detector is detecting the high state or low state. The high state is denoted by '1'and low state is denoted by '0'. The state change modification process depends on the outputs of merging FFs and combinational logic outputs. State Change detector module made up-off XOR gate and OR gate.

III. PERFORMANCES OF PROJECT

In data driven clock gating methodology is used to reduce the power consumption and reduce the delay of the circuit. The data driven clock gating is power reducing using in merging flip flop and integrated clock gating circuit. The block diagram of merging flip flop using data driven clock gating circuit is shown in fig 2. The ICG is disable then the output of state change detector is input of the ICG circuit. State change detector is XORed output and k enabling signal of the Flip Flop, by ORed the input of ICG circuit. The arithmetic circuit is used by logic circuit of data driven clock gating circuit. The merging Flip-flop reduces the unwanted clock signal of circuit. The unwanted glitches are reduced in data driven clock gating circuit.

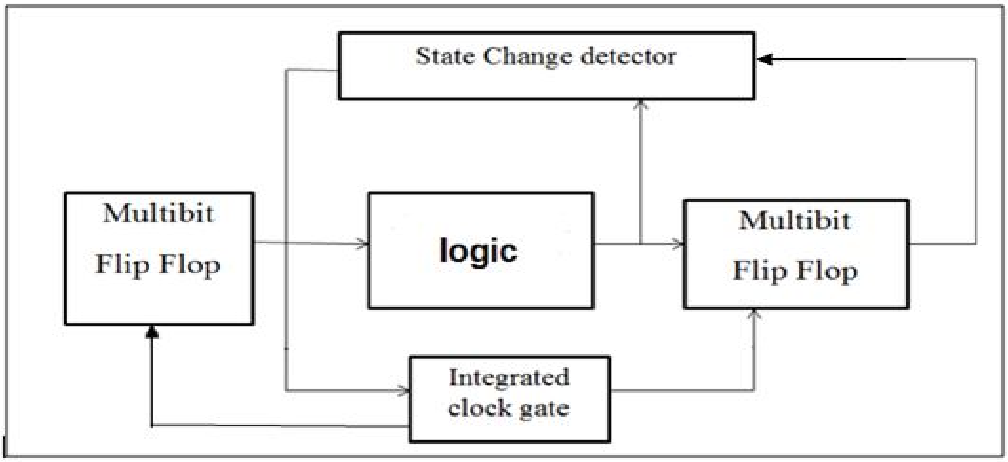

Fig. 2 Block diagram of merging flip flop using data driven clock gating

IV. RESULT AND DISCUSSION

The SYNTHESIS RESULTS of GROUPING FF USING DATA DRIVEN CLOCK GATING using is Xilinx power analyser. Grouping Flip Flop using data driven clock gating Xilinx power report shown in Fig 3.

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Device	
Family	Spartan3e
Part	xa3s250e
Package	tqg144
Grade	Automotive
Process	Typical
Speed Grade	-4

On-Chip	Power (W)	Used	Available	Utilization (%)
Clocks	0.000	2	–	–
Logic	0.000	5	4896	0.1
Signals	0.000	12	–	–
IOs	0.000	8	108	7.4
Leakage	0.052			
Total	0.052			

Supply Summary		Total	Dynamic	Quiescent
Source	Voltage	Current (A)	Current (A)	Current (A)
Vccint	1.200	0.015	0.000	0.015
Vccaux	2.500	0.012	0.000	0.012
Vcco25	2.500	0.002	0.000	0.002

	Total	Dynamic	Quiescent
Supply Power (W)	0.052	0.000	0.052

Environment	
Ambient Temp (C)	25.0
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	0

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	37.5	98.0	27.0

Characterization	
PRODUCTION	v1.2,06-23-09

Fig. 3 Grouping Flip Flop Using Data Driven Clock Gating Synthesis results- Xilinx Power Report

The synthesis result of Merging Flip flop Using Data Driven Clock Gating using is Xilinx power analyser. Merging Flip Flop using data driven clock gating Xilinx power report shown in Fig 3.

Device	
Family	Spartan3e
Part	xc3s100e
Package	vq100
Grade	Commercial
Process	Typical
Speed Grade	-4

On-Chip	Power (W)	Used	Available	Utilization (%)
Clocks	0.000	2	–	–
Logic	0.000	4	1920	0.2
Signals	0.000	9	–	–
IOs	0.000	6	66	9.1
Leakage	0.034			
Total	0.034			

Supply Summary		Total	Dynamic	Quiescent
Source	Voltage	Current (A)	Current (A)	Current (A)
Vccint	1.200	0.008	0.000	0.008
Vccaux	2.500	0.008	0.000	0.008
Vcco25	2.500	0.002	0.000	0.002

	Total	Dynamic	Quiescent
Supply Power (W)	0.034	0.000	0.034

Environment	
Ambient Temp (C)	25.0
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	0

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	49.0	83.4	26.6

Characterization	
PRODUCTION	v1.2,06-23-09

Fig. 4 Merging FFs using data driven clock gating -Xilinx power

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Table 1. Comparison of Grouping FFs using Data Driven Clock Gating Vs Merging FFs using Data Driven Clock Gating

Parameters	Grouping FFs using Data Driven Clock Gating	Merging FFs using Data Driven Clock Gating
Power Consumption	52mW	34mW
Delay	2.394ns	2.450ns

The comparison of Grouping FFs using Data Driven Clock Gating Vs Merging FFs using Data Driven Clock Gating shown in table 1 the power and delay are measure by Xilinx power analyser.

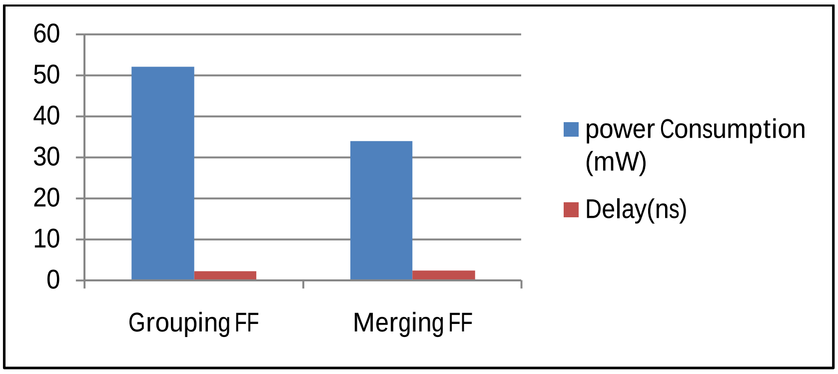

Fig. 5 Flow chart report of power consumption and delay

The Flow chart report of power consumption and delay in Grouping FFs using Data Driven Clock Gating Vs Merging FFs using Data Driven Clock Gating shown in fig 5.

VI.CONCLUSION

The objective of the system is to reduce the area, delay & power of data driven clock gating technique. In proposed method using merging FFs for combined clocking by a shared gater to yield highest dynamic power savings. Analysed, the results of grouping and merging FFs architectures, simulation and synthesis. As the result of the area, delay parameters, grouping FF using data driven clock gating is more effective than the merging FF using data driven clock gating. In case of grouping FFs using data driven clock gating is 30% extraordinary power saving for merging FFs using data driven clock gating.

In this paper, analysis between grouping FFs using data driven clock gating and merging FFs using data driven clock gating. Furthermore, real time application of DSP cores, a network processor control block, and a 3-D graphics accelerator using in merging FFs using data driven clock gating in an attempt to yield further power savings.

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BIOGRAPHY

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