



# Reversible Gate Based Testable Sequential Circuits

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**ABSTRACT:** Testing of Sequential circuits can be done by two test vectors (all 1's and all 0's) if the circuits were based on the conservative logic. The circuit is made to be tested by designing the circuit with the help of Reversible logic gates. Fredkin gate is used as reversible gate in this literature. Sequential circuits such as latches, flip flops are designed with the help of conservative logic reversible gate which are coded by modelsim and simulated in this paper. So, testing does not require any scan path access to the internal memory cell, since only normal mode and test mode are required for testing by all zeros and all ones. The objective of this paper is to reduce the number of test vector thereby testing time can be reduced. Thereby Fault coverage is achieved.

**KEY WORDS** – Conservative logic, Reversible gate

## I. INTRODUCTION

Conservative logic is a logic which reflects the property that there is equal number of one's in the inputs as well as in the outputs[1]. It can be reversible or irreversible in nature. Reversibility is nothing but the circuit exhibits one-to-one mapping between input and output vector, and also represents for each input vector there is an unique output vector and vice versa. Conservative logic is said to be reversible only when the circuit possess the above property of reversibility. Otherwise, conservative logic is irreversible. Reversibility is mainly preferred because it can provide the methodology for designing low power circuits. Any sequential circuit can be tested by having only two test vectors (all 1's and all 0's) when the circuit is based on conservative logic. The designs of latches, flip flops are presented based on reversible conservative logic gate.

There are number of existing reversible logic gates such as Fredkin gate, Feynman gate, Peres gate, Toffoli gate. Fredkin gate is used for designing such testable sequential circuit is presented, thereby avoiding the usage of scan path access to the internal memory cell [2]. Henceforth, testing time can be reduced. Testable sequential circuit can have normal mode and test mode. In the normal mode, the circuit will have feedback but in the test mode, the circuit is made as suitable by disrupting the feedback. So, the circuit is to be tested by only two test vectors (0's and 1's).

This paper involves: Section II represent the fundamentals such as Reversible Fredkin gate, and the Conservative logic. Section III represents testable sequential circuits such as reversible gate based latch and reversible gate based flip flops. Section IV shows the simulation results and Section V represents the conclusion.

## II. FUNDAMENTALS

### Reversible fredkin gate

Reversible gate is a logical gate with one-to-one mapping i.e., for each input vector, there is a unique output vector and vice versa. Also known as reversible conservative logic. Fanout at the output is not allowed. The designs presented in this paper are based on conservative reversible (three inputs: three outputs) Fredkin gate shown it can be described as mapping  $(A, B, \text{ and } C)$  to  $(P = A, Q = AB + AC, \text{ and } R = AB + AC)$ , where  $A, B, \text{ and } C$  are the inputs, and  $P, Q, \text{ and } R$  are the outputs, respectively. The operation involves: Whenever the first input (say  $A$ ) is 1, the swapping of inputs  $B$  and  $C$  is done at the output. Otherwise, output is same as input. Table I shows the truth table of Fredkin Gate, and it can be seen that

Fredkin gate produces the same number of 1's in the outputs as on the inputs, in addition to the one-to-one mapping feature of reversibility.

**Conservative logic**

A conservative-logic gate is any Boolean function that is invertible and conservative. It is well known that, under the ordinary rules of function composition (where fan-out is allowed), the two-input NAND gate constitutes a universal primitive for the set of all Boolean functions. In conservative logic, an analogous role is played by a single signal-processing primitive, namely, the Fredkin gate, defined by the truth table.

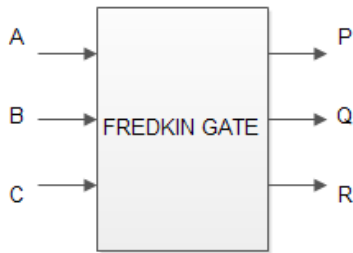


Figure 1 Fredkin gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

Table I Truth table of Fredkin gate

This computing element can be visualized as a device that performs conditional crossover of two data signals according to the value of a control signal. When the control signals, say A is 1, swapping of B and C is done and is reflected at the output. Otherwise, Output is same as that of input only when A is 0. Observe that the Fredkin gate is nonlinear and coincides with its own inverse. Any output of a gate can be connected only to the input of a wire, and similarly any input of a gate only to the output of a wire.

**III. TESTABLE SEQUENTIAL CIRCUITS: LATCHES AND FLIP FLOPS**

The sequential circuits are made suitable to be tested by only two test vectors. Fredkin gate is used to design those sequential circuits[5]. Therefore the circuit is suitable for testing thereby scan path access is not required and testing time is reduced finally. Sequential circuits say Latches and flip flop (DET flip flop and Master-Slave flip flop) are considered.

**Reversible gate based D Latch**

Latch is the basic element used to store the data in digital design. Sequential circuits are mainly preferred because of its memory. D latch is considered in this paper, designed by using reversible gate say the fredkin gate and tested by all zero's and all one's shown in the figure 2. This is coded by the VHDL language and then simulated. This circuit involves normal mode and test mode.

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In the Normal mode, control signals (say C1 and C2) are set to 01. Then the sequential circuit will operate as D latch without any fan-out problem. Test mode involves control signals which are set to C1C2=00 (all 0's). So that the design can be tested with the respective vector. Thus stuck at 1 fault can be detected. It is same as that for the stuck at 0 faults to be detected; both the C1 and C2 are set to 11. Then the design will disrupt the feedback in test mode and take care of the fanout.

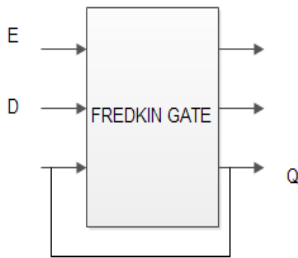


Figure 2 Reversible gate based D Latch.

The Reversible gate based circuit with the respective control signals are shown in the figure 3,4,5. Unidirectional stuck at fault are then detected. These two test vectors are long enough to detect all faults present in the circuit.

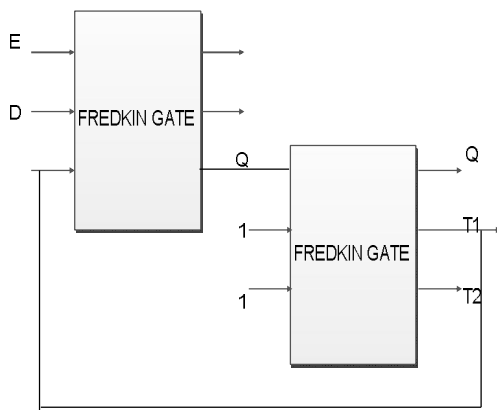


Figure 3 In test mode by passing test vector of all 1's of all 0's

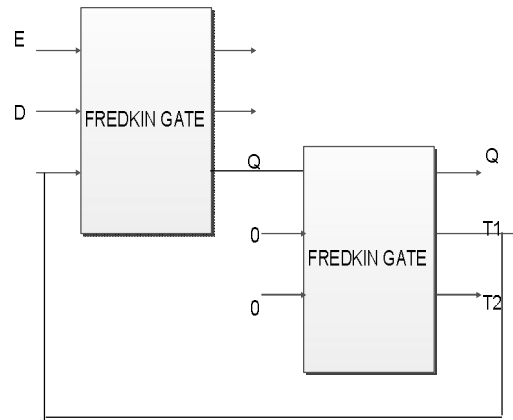


Figure 4 In test mode by passing test vector

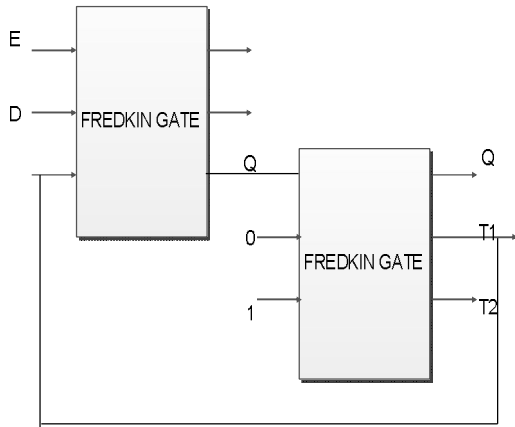


Figure 5 Design under normal mode

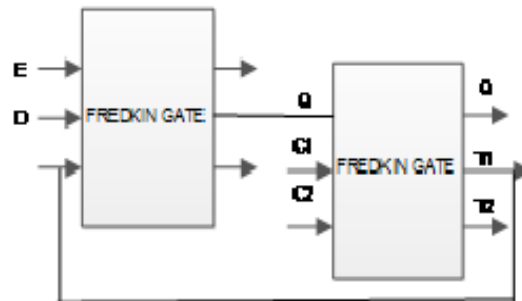


Figure 6: Negative enable fredkin gate based D latch

The negative enable D latch is also coded and tested by using the test vectors. It is illustrated in the figure 6. This latch is activated only when the enable is negative or  $E=0$ . In this design, the second fredkin gate will take care out of the fan out and the design can be tested.

### Reversible gate based Master slave D flip flop

Flipflop is another storage element used to store one bit of information. The only difference between latch and flip flop is that enable signal. Flip flops such as Master-slave flip flop and DET flipflop are considered to design the testable sequential circuits Fredkin gate is used in order to make the design to be tested by two test vectors. Like the Reversible gate based D latch, this design consists of normal mode and test mode. Hence the faults are detected and the testing time is reduced rather than the designs are tested using the scan path. For the Master slave D flip flop, the figure 7 represents

consist of Positive enable D latch acts as master and slave where the negative enable D latch is acts as slave. The control signals mc1, mc2, sc1 and sc2 are set to 01. The control signals are set to 01 for the normal mode.

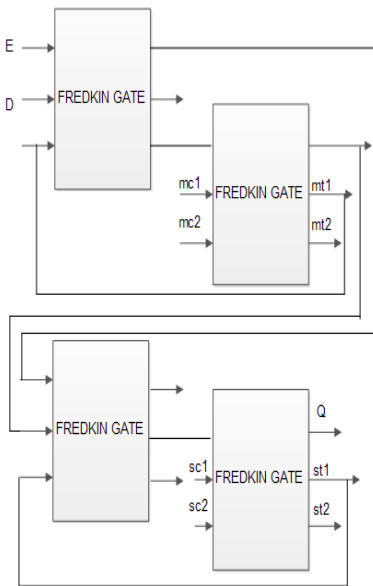


Figure 7 Reversible gate based Master slave D flipflop

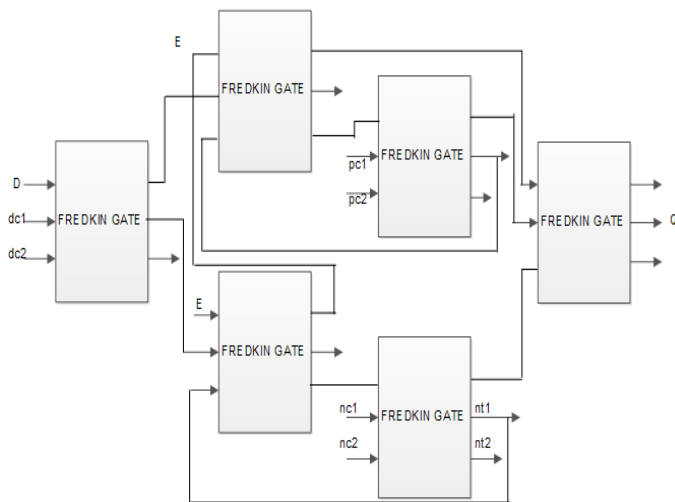


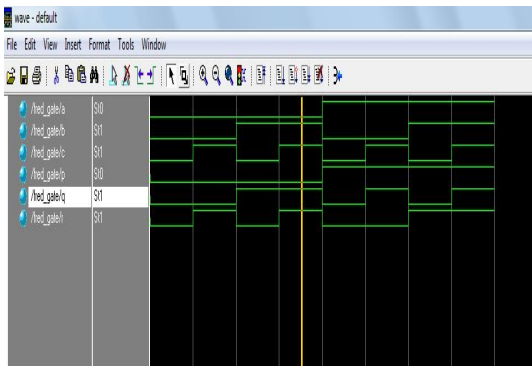
Figure 8 Reversible gate based DET flipflop

In the test mode, all the stuck at 0 fault can be detected by setting the control signals(mc1,mc2,sc1,sc2) to 1111.Likewise, all the stuck at 1 fault can be detected by passing the test vector of all zeros (i.e.)0000.D flipflop is considered for this design because the output is preserved from its input. The wholesome design can be implemented using the fredkin gate since it is a reversible gate. The reason is that reversible gate exhibits low power dissipation compared to the CMOS. Both the test vectors 0000 and 1111 will break the feedback in the test mode.

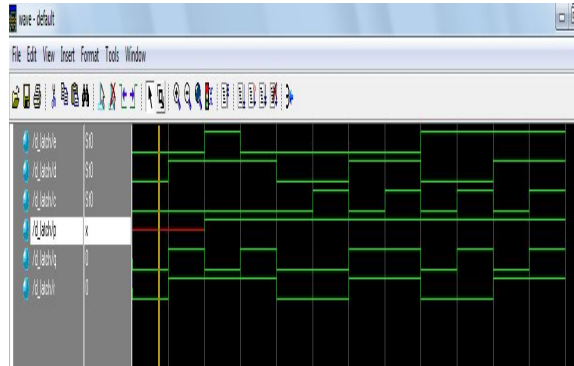
### Reversible gate based DET flipflop

The above design method is same as that for designing the DET flipflop which is coded and simulated by modelsim. In the Master slave flipflop, the sampling and storing the input data at both positive and negative edges (the rising and the falling edge) of the clock cannot be possible. In order to overcome this, DET flipflop is used (illustrated below). The advantage of this design is that the data rate can be maintained and frequency is reduced to half when compared with the master slave flipflop.This design is illustrated above(figure 8). The design consists of positive enable and negative enable flipflop along with the 2:1 mux at the output to pick one of the results from the design. Both the positive enable flipflop, negative enable flipflop are in parallel but the fan out is not allowed since it is reversible and control signals such as pc1,pc2,nc1,nc2. The same procedure is applied for the test mode and normal mode.

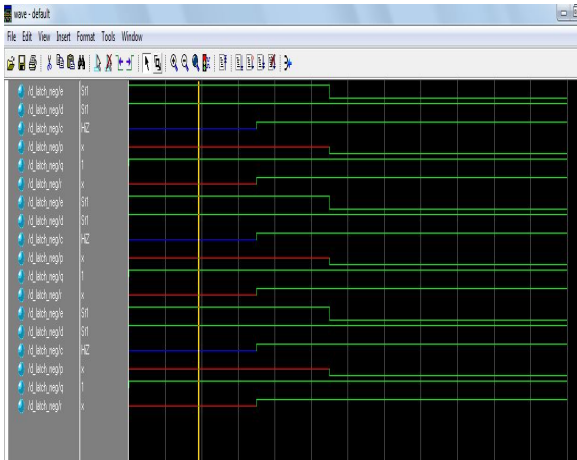
## IV SIMULATION RESULTS



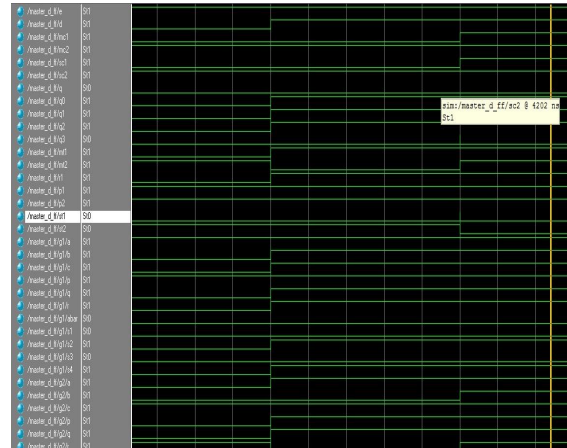
Fredkin gate



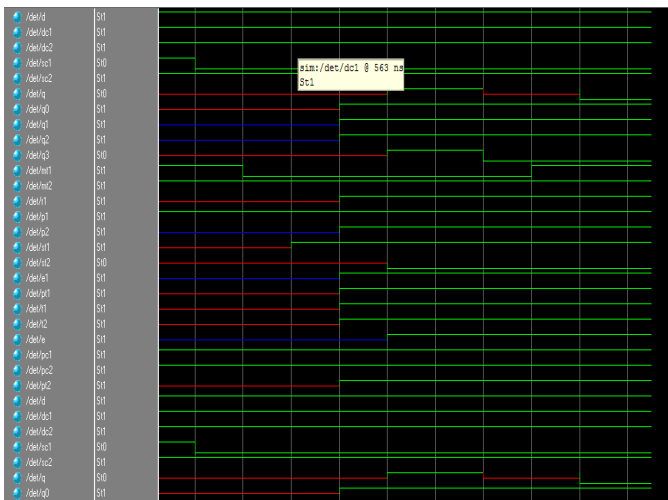
Fredkin gate based D latch



Fredkin gate based negative enable D latch



Reversible gate based master slave D flipflop



Reversible gate based DET flipflop

## V. CONCLUSION

Sequential circuits are basically used for testing. Instead of scan path access to the internal memory cell, the circuits are designed by the reversible gate especially fredkin gate. The designs of reversible gate based latch, flipflop are made. Since those circuits are based on conservative logic and the circuits are made to be changed by reversible gates, the entire design can detect all possible stuck at 1 fault that can be found by having test vector of all zero whereas all possible stuck at zero fault can be found by all ones. Thereby, testing time may be reduced to some extent.



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