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Signal Flow Graph Realization of Higher-Order Current-Mode All Pole Low-Pass Filters Using Five Current Follower Transconductance Amplifiers (CFTAs)

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Research Article

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ABSTRACT

Objective: Signal flow graph realization of higher-order current-mode all-pole low-pass current transfer functions with five Current Follower Transconductance Amplifiers (CFTAs) is presented. The fifth presented filters with one input and three outputs employ five CFTAs and five capacitors, and it can simultaneously realize third order low pass, fourth-order low pass, and fifth-order low pass current responses, from the proposed circuit topologies. Bipolar and CMOS technologies are used for CFTA implementation. This study aims to provide a literature survey for identifying research gaps and to design and implementation of the Current follower Transconductance Amplifier (CFTA) with constant gm demonstrated. To implement the CFTA active device in the bipolar technology structure depicted in CFTA which has been employed using transistor model parameters PR100N (PNP) and NP100N (NPN) of the bipolar arrays ALA400 and the COMS technology structure using, 0.5 μm CMOS process parameters for nMOS and pMOS transistors.

Methods: The approach had been based on drawing a signal flow graph directly from the given transfer function and then obtaining, from the graph, the Active-C filter involving CFTAs. Third-order Butterworth low-pass circuit requires only three CFTAs and three grounded capacitors, fourth-order Butterworth low-pass circuit requires only four CFTAs and four grounded capacitors and fifth-order Butterworth low-pass circuit require only five CFTAs and five grounded capacitors. One Filter based on input and output is characterized by its transfer function. The transfer function of a filter is the ratio of the output signal to that of the input signal as a function of the complex frequency. The obtained filter characteristics include the natural frequency (ωo) and the quality factor (Q-factor) which are electronically tuned through biasing current of the transconductance gain of the CFTAs. The resulting circuits obtained from the synthesis procedure are resistor-less structures and are especially suitable for monolithic implementation. The circuits also have low sensitivity characteristics and exhibit electronic controllability coefficients via transconductance gains (gm) of CFTAs.

Results: To demonstrate the proposed approach, the third-order, fourth-order, and fifth Butterworth all-pole low-pass filters were designed and simulated using MATLAB Simulink. Conclusion: The study of the simulation of the third-order, fourth-order, and fifth-order all-pole low-pass filters has been carried out. The CFTA circuits have been simulated using MATLAB SIMULINK. The simulation results are in agreement with the theory.

INTRODUCTION

The current Follower Transconductance Amplifier (CFTA) has been introduced in Biolek D [1]. This current input and output

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building block is particularly useful in realizing analog signal processing functions requiring explicit current outputs. The CFTA is slightly modified from the conventional Current Differencing Transconductance Amplifier (CDTA) [2] by replacing the current differencing unit with a current follower and complementing the circuit with a simple current mirror for copying the z-terminal current. CFTA is a composite of a CF usually realized from a translinear CCII, a Current Conveyor Transconductance Amplifier (CCTA) has directly a CCII followed by an OTA [3]. The CFTA element is a combination of the current follower and the multioutput operational transconductance amplifier. Consequently, there are several structures for realizing the current mode of active filters using CFTAs [4]. However, the work had been studied in the synthesis of the general nth-order all-pole lowpass transfer function. Also, the realization of an nth-order lowpass filter using current conveyors was introduced in Gunes EO [5] the circuit has too many grounded resistors, i.e. (n+1) current conveyors, n grounded resistors and n grounded capacitors. Therefore, this work largely focuses on presenting a general synthesis procedure for the realization of the Nth-Order all-pole low pass Transfer function. The approach is based on drawing a signal flow graph directly from the given transfer function and then obtaining, from the graph, the Active-C filter involving CFTAs. The resulting circuit uses a minimum number of n CFTAs and n grounded capacitors, which makes the circuit especially suitable for monolithic implementation. It is shown that the design procedure proposed here is general and simple. Simulation results from MATLAB Simulink illustrate the properties of the proposed design procedure.

In this present study, the recent work of Dike is extended to include the active building block Current Follower Transconductance Amplifier (CFTA) and its basic applications like amplifiers, grounded and floating inductors and active filters in analog signal processing. Designed examples and computer simulations by Matlab Simulink confirm the usefulness of the proposed approach. Its various instrumental applications are filter and conventional controllers (proportional, integral and derivative). These CFTA based conventional controllers are studied and their characteristics are analysed through computer simulation and verified in Matlab Simulink.

Literature Review

Bipolar and CMOS technologies are used for CFTA implementation. One of the CFTA realizations using bipolar technology is reported in Herencsar N [6]. The advantage of these circuits is high overall gain compared to CMOS based implementations. A high gain, these CFTA structures also produce high power dissipation due to the use of leakages in BJT. Another bipolar implementation which is an extension of CFTA known as ZC-CFTA is presented in Tangsrirat W [7]. In this structure, an extra z-terminal termed as z-copy is included to provide design flexibility. A Current-Controlled CFTA (CCCFTA) based on BJT technology is presented in Jaikla W [8]. In this structure, the input voltages of f-terminals is zero and therefore these terminals have a finite resistance that can be controlled through bias currents [9-11].

CMOS is also sometimes referred to as complementary-symmetry metal-oxide-semiconductor. The words “complementary-symmetry” refer to the fact that the typical digital design style with CMOS uses complementary and symmetrical pairs of p-type (PMOS) and n-type (NMOS) metal oxide semiconductor field-effect transistors (MOSFETs) for logic functions. CMOS technology-based CFTA structures has also been reported in the literature. One such structure is reported in Chauhan AS [11] which has an advantage of high impedance at the z-terminal. A low power CMOS realization of the CFTA is reported in Li YA [12]. In this structure, the input stages are constructed using FVF, due to which this CFTA has very low input resistance. The modification of CFTA known as CC-CFTA is reported in Herencsar N [3] which has the advantage of better OTA gain and multiple outputs can be drawn out of CFTA. Another CMOS based CFTA is reported in Herencsar N [13]. This circuit exhibit very low impedance at the inputs and high (typically in GΩ). A comparison of available CFTA structures in terms of supply voltage, technology and number of transistors, gain, power dissipation, and terminal impedances is presented in **Table 1**.

Table 1. Bipolar realization of CFTA.

Reference	Technology	Supply voltage	Bais current	Transconductance gain	Power dissipation
Tangsirat et al.	Bipolar	± 3 V	100 µA	2 mS	-
Lahiri et al.	Bipolar	± 2.5 V	50 µA	0.96 mS	-
Jaikla et al.	Bipolar	± 1.5 V	100 µA	-	8.11 mW
Tangsrirat et al.	0.35 µCOMS	± 2.5 V	10 µA	-	0.43 mW
Herencsar et al.	0.5 µCOMS	± 1.85 V	400 µA	-	10.6 mW
Singh et al.	0.25 µCOMS	± 0.75 V	40 µA		0.6 mW

Bipolar-based CFTA circuit realization suitable for the monolithic IC fabrication is displayed in **Figure 1**.

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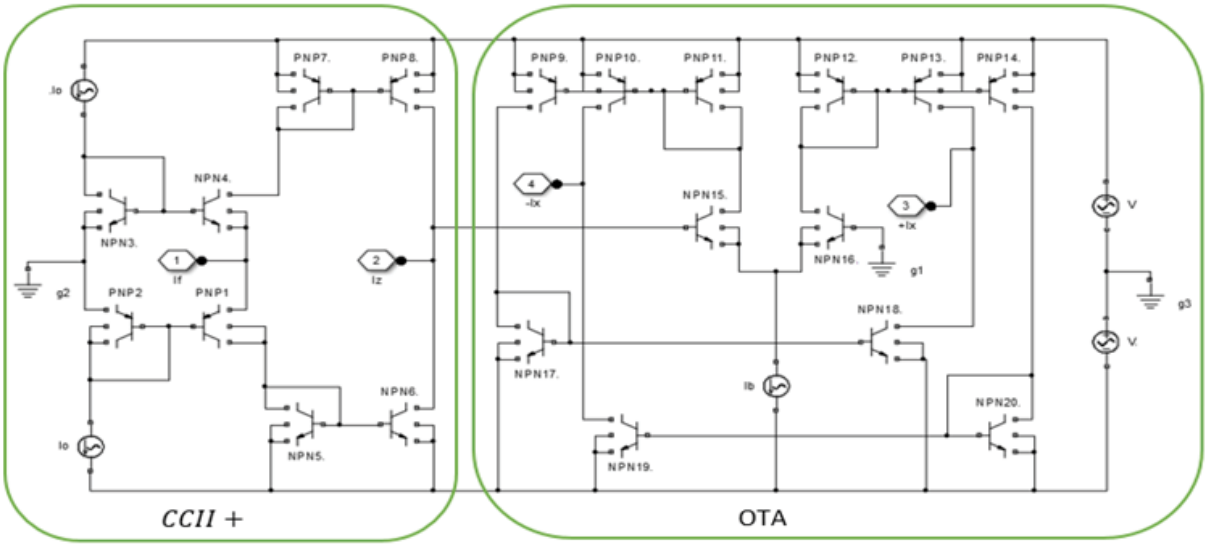

Figure 1. Bipolar realization of the CFTA.

Bipolar realization of the CFTA used in this work is shown in **Figure 1**. The circuit consists of a current conveyor circuit Q1-Q8 and operational transconductance amplifier Q9-Q20. Therefore, in this case, the transconductance gain $g_m = \frac{I_B}{2V_T}$ is directly proportional to the external bias current IB, which can be written as where $V_T \cong 26$ mV at 27 °C is the thermal voltage.

CMOS Realization of CFTA

CMOS-based CFTA circuit realization suitable for the monolithic IC fabrication is displayed in **Figure 2**.

CMOS realization of the CFTA used in this work is shown in **Figure 2**. The circuit consists of a current conveyor circuit Q1-Q8 and operational transconductance amplifier Q9-Q20. Therefore, in this case, the transconductance gain of CMOS based 1th CFTA (i=1,2,3), can be controlled through the biasing current I_{Bi} which can be written as $g_m = \sqrt{\beta_o I_{oi}}$ where $\beta_o = \mu_o C_{ox} \frac{W}{L}$ is the process parameter, is the free electron mobility in the channel, is the gate oxide capacitance per unit area, W and L are the channel width and length respectively.

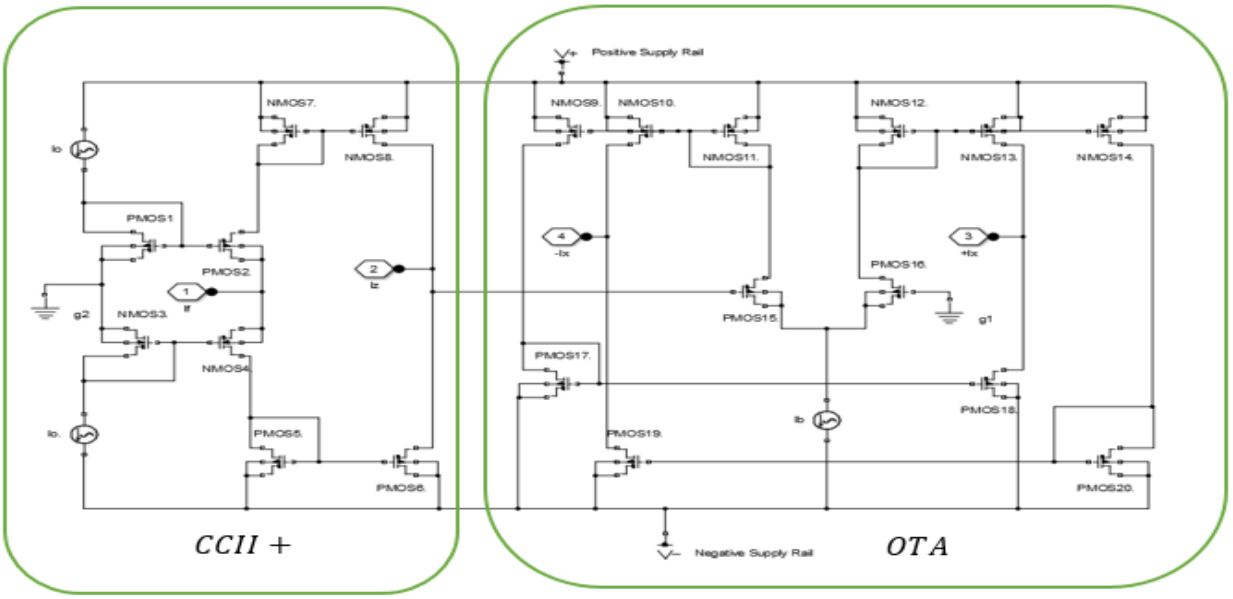

Figure 2. CMOS realization of the CFTA.

LITERATURE SURVEY

In the past few decades, the current mode (CM) analog signal processing has received considerable interest owing to the advantages offered by CM techniques which have been elaborated. This has resulted in the emergence of various CM analog building blocks and CFTA is one among those. The CFTA block was first reported by Biolek D [2]. A Current Follower Transconductance

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Amplifier (CFTA) can be considered to be a reduced version of the CDTA instead of the current-differencing unit as the front end, it has a current follower as the front end which can be easily implemented from a CCII+ by grounding its Y-terminal. The operation of the CCII current conveyor is such that if Current conveyor (CCII+) is constructed by a Voltage Follower (V_F) between the Y-terminal and the X-terminal in order to accomplish $v_x=v_y$, and a Current Mirror (CM) between the X-terminal and the Z-terminal in order to accomplish $i_z=i_x$ [14]. The block diagram of the CFTA can be drawn as shown in **Figure 3a**. Thus, it is a four-terminal building block having one input terminal f and three outputs terminals Z, x+ and x-. The output current entering into terminal Z is the same as the one entering into the low impedance terminal f, whereas when terminal Z is terminated into an impedance, two complimentary output currents are available as i_{+x} and i_{-x} which are respectively given by $i_{+x}=g_m v_z$ and $i_{-x}=-g_m v_z$. A CC-based implementation of the CFTA is shown in **Figure 3b** which can also be considered to be a special case of the CDTA with input terminal n being grounded [12].

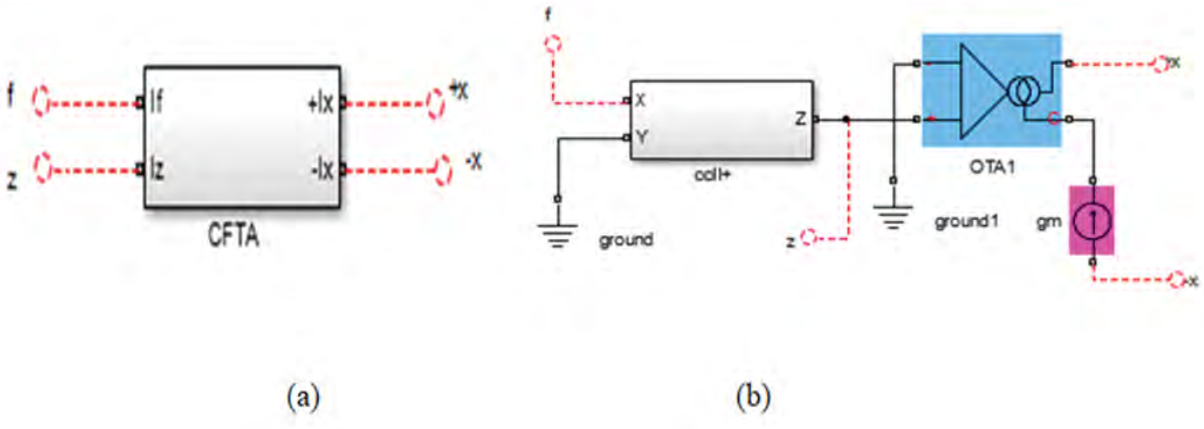

Figure 3. CFTA realization (a): block diagram implementation; (b): Implementation of the CFTA using CCII and OTA.

MATHEMATICAL MODEL

This current input and output building block is particularly useful in realizing analog signal processing functions requiring explicit current outputs. The symbolic representation of the CFTA and its behavior model are shown in **Figure 4**. Assuming the standard notation, the terminal defining relations of this device can be characterized by the following set of equations [4].

$V_f=0,\ i_z=i_f,\ i_x=g_m v_z=g_m Z_z i_z$

where g_m is the transconductance gain of the CFTA and Z_z is an external impedance connected to the *z*-terminal. The CFTA consists essentially of the current follower at the input port and the multi-output transconductance amplifier at the output part. According to Biolek D [1] and **Figure 4**, the *f*-terminal forms the current input terminal at ground potential ($V_f=0$) and the output current at the *z*-terminal (i_z) follows the current (if) through the *f*-terminal. The voltage drop at the *z*-terminal (V_z) is then converted to a current at the *x*-terminal (i_x) by a g_m-parameter. In general, the g_m-value is adjustable over several decades by a supplied bias current/voltage, which lends electronic controllability to design circuit parameters. It is seen that the graph consists of two basic operations, which are current summation and current lossless integrator, as redraw in **Figures 5b and 6c**, respectively. In most of the applications, the z terminal of a CFTA element connected by grounded load impedance Z. Special Signal Flow Graphs (SFGs) can be used in such circuits for their analysis and synthesis; these are called "IVI" (Current-Voltage-Current) Signal Flow Graphs. **Figure 3a** shows the "IVI" SFG of the CFTA element. As shown in **Figure 5b**. SFG can be simplified by removing the intermediate voltage node. Using the current and voltage relations of the CFTA given in equation (1),

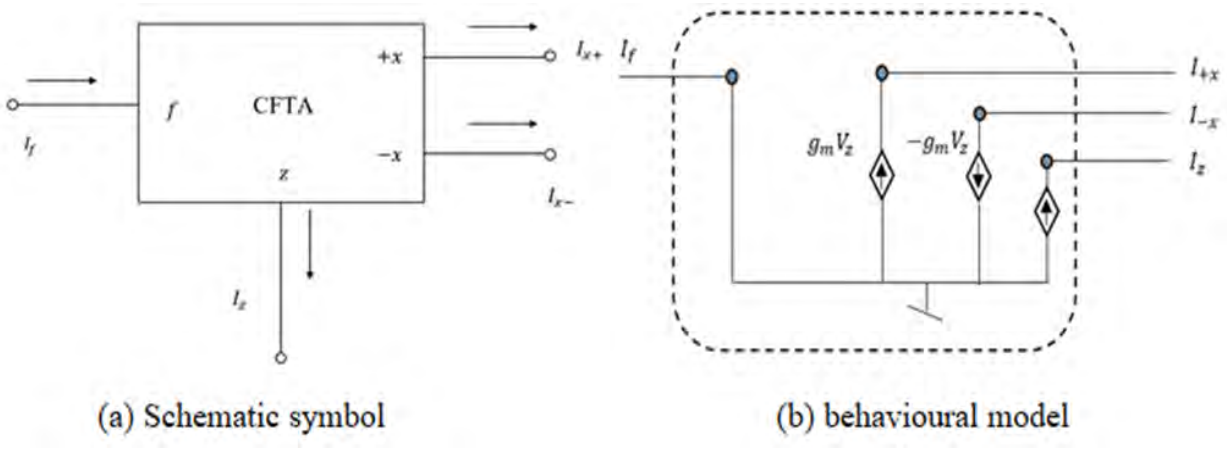

Figure 4. The CFTA.

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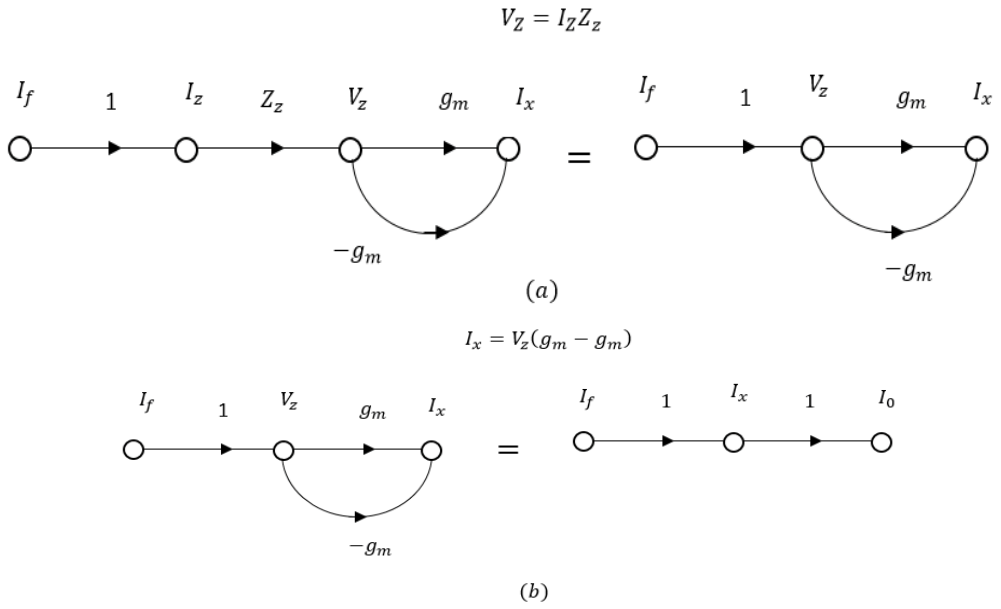

Figure 5. Signal flow graphs (a): cascade transformation and; (b): parallel transformation.

We can easily find that these two sub-graphs also can be realized using CFTA by the sub-circuits shown in **Figures 4b and 6a**, respectively.

Using Kirchhoff's current law (KCL). We get

If+sCVz=sτIz

Where $I_z=I_f$, $I_z=g_m$ and $\tau = \frac{c}{g_m}$

$$I_z + sCV_z = \frac{sCI_z}{g_m} \Rightarrow V_Z = \frac{I_z}{g_m} - \frac{I_z}{sC} \Rightarrow I_z = I_z\left(1 - \frac{g_m}{sC}\right) = s\tau I_z \quad (1)$$

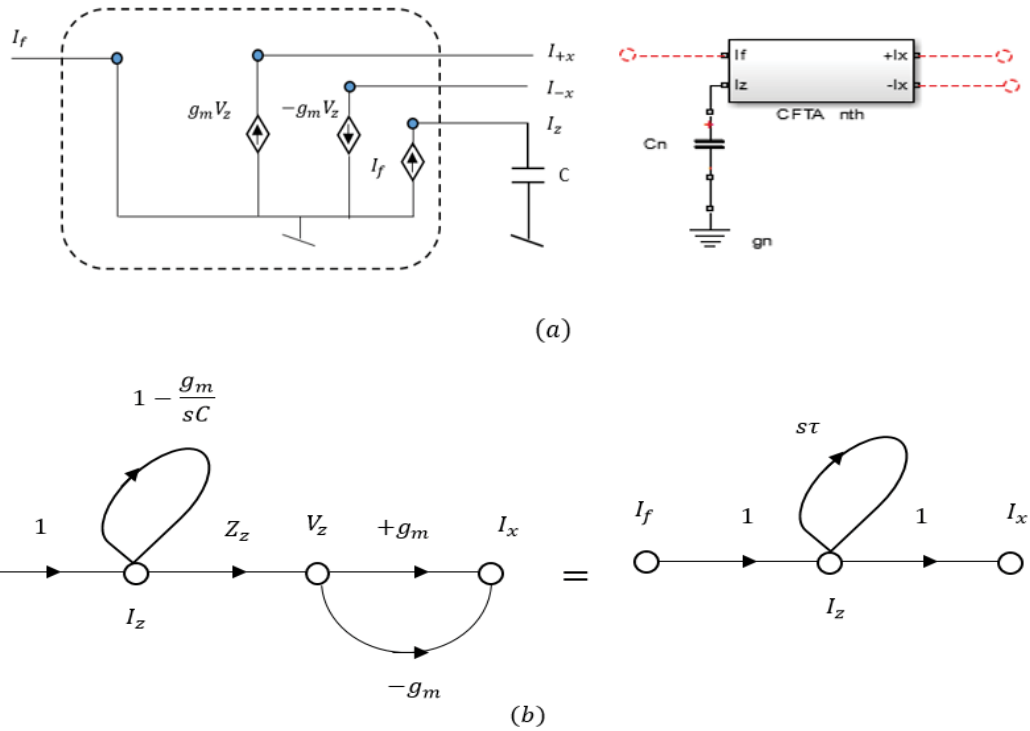

Figure 6. Sub-graphs and their corresponding Active-C sub-circuits involving CFTAs.

For the CFTA-based realization, it can readily obtain the CFTA-C circuit by interconnecting the corresponding sub-circuits of **Figure 6a** according to the overall signal flow representation of **Figure 7**. The CFTA-C circuit realizing any nth-order low-pass

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current transfer function is shown in **Figure 7**. For this realization, it has to be noted that the proposed filter configuration contains n CFTAs as active elements and n capacitors as passive elements for general nth-order filter function. Also, note that the circuit realization uses only grounded capacitors that are suitable for the integrated circuit point of view [15] and also provides low-input impedance and high-output impedance terminals that are desirable for cascading in current-mode [16,17]. We can see that the low input impedance f terminal of each CFTA is connected to high output impedance ± x terminals of other CFTA. Parasitic impedances are connected between true ground node f and virtually grounded node f. Therefore, these are almost ineffective. As a result, The parasitic impedances of –x terminal of CFTA-1 at node 1, +x terminal of CFTA-1 at node 2, -x terminal of CFTA-2 at node 1, +x terminal of CFTA-2 at node 3 and –x terminal of CFTA-3 at node 1 +x terminal of CFTA-3 at node 4 and –x terminal of CFTA-4 at node 1 +x terminal of CFTA-4 at node 5 and –x terminal of CFTA-n at node 1, 1 +x terminal of CFTA-n at node n are almost ineffective. The only parasitic impedances for consideration are z_1, z_2, z_3, z_4...and z_n across external capacitors C_1, C_2, C_3, C_4... and C_n connected between high impedance z terminal and ground of CFTA-1, CFTA-2, CFTA-3, CFTA-4... and CFTA-n.

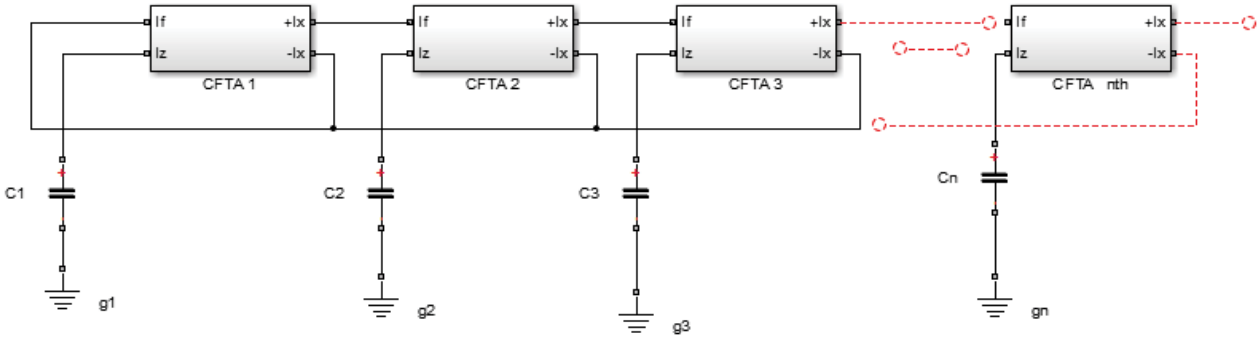

Figure 7. CFTA-based realization of the n-order current-mode low-pass filter, corresponding to the SFG given in **Figure 6**.

The above expression can be represented by the signal flow graph (SFG) as shown in **Figure 6**

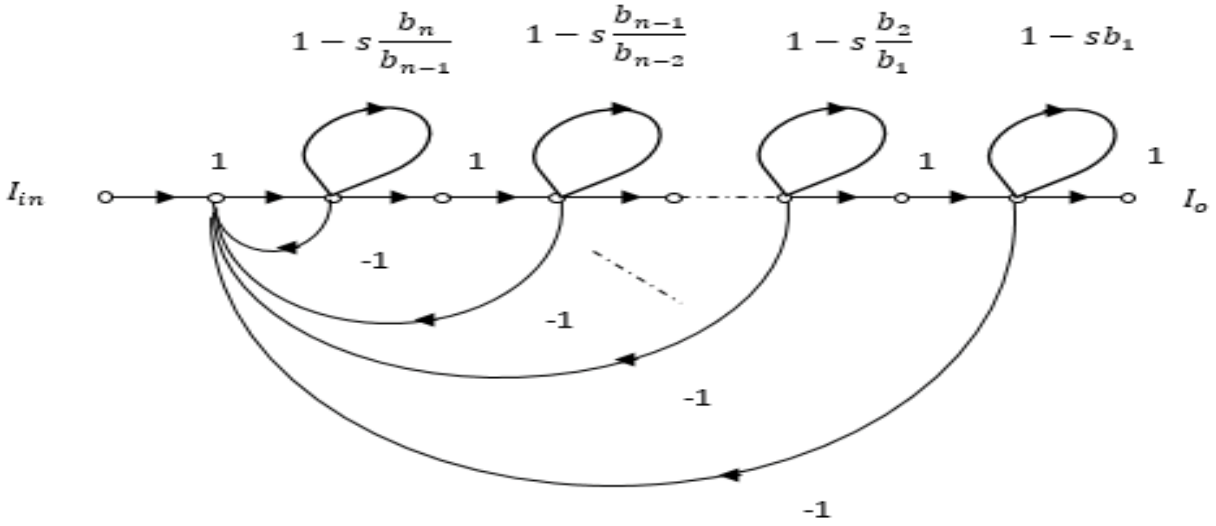

Figure 8. Signal flow graph representing equation (2).

The corresponding set of equations are:

$I_1=I_{in}-I_2-I_3-\ldots-I_6-I_7$

$$I_2 = I_1 - \left(1 - \frac{sb_n}{b_{n-1}}\right) I_2 \Rightarrow I_2 \frac{sb_n}{b_{n-1}} = I_1$$

$$I_3 = I_2 - \left(1 - \frac{sb_n}{b_{n-1}}\right) I_3 \Rightarrow I_3 \frac{sb_n}{b_{n-1}} = I_2$$

$$I_4 = I_3 - \left(1 - \frac{sb_n}{b_{n-1}}\right) I_4 \Rightarrow I_4 \frac{sb_n}{b_{n-1}} = I_3$$

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$$I_5 = I_4 - \left(1 - \frac{sb_n}{b_{n-1}}\right) I_5 \Rightarrow I_5 \frac{sb_n}{b_{n-1}} = I_4$$

$$I_6 = I_5 - \left(1 - \frac{sb_n}{b_{n-1}}\right) I_6 \Rightarrow I_6 \frac{sb_n}{b_{n-1}} = I_5$$

$I_7=I_6-(1-sb_1)I_7 \Rightarrow I_7\, sb_1=I_6$

$I_{out}=I_7$ and I_{in} represent a source node, I_{out} a sink node.

The denominator of a filter transfer function determines the poles and the fall-off rate of the frequency response. The denominator of the biquadratic function has the same form for all types of filters. The general form of an n-order lowpass current transfer function can be expressed by the following formula :

$$\frac{I_o(s)}{I_{in}(s)} = \frac{1}{b_n s^n + b_{n-1} s^{n-1} + ... + b_2 s^2 + b_1 s + 1} \quad (2)$$

From the realization of **Figure 7**, the design equations can be obtained by comparing **Figure 5b** with **Figure 8**. The results are summarized as follows:

$$\frac{b_n}{b_{n-1}} = \frac{c_1}{g_{m1}}$$

$$\frac{b_{n-1}}{b_{n-2}} = \frac{c_2}{g_{m2}}$$

....

$$\frac{b_2}{b_1} = \frac{c_{n-1}}{g_{m(n)}}$$

$$b_1 = \frac{c_n}{g_{m(n)}} \quad (3)$$

It should be noted from the above expressions that the coefficients bi (i=1,2,3,4,5 ...,n) of the realized function can be tuned electronically by adjusting the g_m value of the CFTA.

MATERIALS AND METHODS

In the proposed circuit topologies in **Figure 9**. we can see that the low impedance f terminal of each CFTA is connected to high impedance ± x terminals of other CFTA. This use of current feedback minimizes or eliminates the possibilities of parasitic impedance effects of CFTAs to be considered. A practical CFTA, to any other element, includes various ports parasitic as shown in **Figures 9-14**.

Third-Order Butterworth Low Pass Filter

Parasitic impedances are connected between true ground node f and virtually grounded node f. Therefore, these are almost ineffective. As a result, The parasitic impedances of –x terminal of CFTA-1 at node 1, +x terminal of CFTA-1 at node 2, -x terminal of CFTA-2 at node 1, +x terminal of CFTA-2 at node 3 and –x terminal of CFTA-3 at node 1 are almost ineffective. The only parasitic impedances for consideration are z_1, z_2 and z_3 across external capacitors C_1, C_2, and C_3 connected between high impedance z terminal and ground of CFTA-1, CFTA-2, and CFTA-3.

Fourth-Order Butterworth Low Pass Filter

Parasitic impedances are connected between true ground node f and virtually grounded node f. Therefore, these are almost ineffective. As a result, The parasitic impedances of –x terminal of CFTA-1 at node 1, +x terminal of CFTA-1 at node 2, -x terminal of CFTA-2 at node 1, +x terminal of CFTA-2 at node 3 and –x terminal of CFTA-3 at node 1 +x terminal of CFTA-3 at node 4 and –x terminal of CFTA-4 at node 1 are almost ineffective. The only parasitic impedances for consideration are z_1, z_2, z_3 and z_4 across external capacitors C_1, C_2, C_3 and C_4 connected between high impedance z terminal and ground of CFTA-1, CFTA-2, CFTA-3, and

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CFTA-4.

Fifth-Order Butterworth Low Pass Filter

Parasitic impedances are connected between true ground node f and virtually grounded node f. Therefore, these are almost ineffective. As a result, The parasitic impedances of –x terminal of CFTA-1 at node 1, +x terminal of CFTA-1 at node 2, -x terminal of CFTA-2 at node 1, +x terminal of CFTA-2 at node 3 and –x terminal of CFTA-3 at node 1 +x terminal of CFTA-3 at node 4 and –x terminal of CFTA-4 at node 1 +x terminal of CFTA-4 at node 5 and –x terminal of CFTA-5 at node 1 are almost ineffective. The only parasitic impedances for consideration are z_1, z_2, z_3, z_4 and z_5 across external capacitors C_1, C_2, C_3, C_4 and C_5 connected between high impedance z terminal and ground of CFTA-1, CFTA-2, CFTA-3, CFTA-4 and CFTA-5.

EXPLANATION OF LOW PASS FILTERS

Third-Order Butterworth Lowpass Filter

Third-order all-pole low pass Butterworth current transfer function. It can easily show that this transfer function can be represented by the signal flow graph shown in **Figure 9a**, and the corresponding circuit realization of this graph is thus shown in **Figure 9b**.

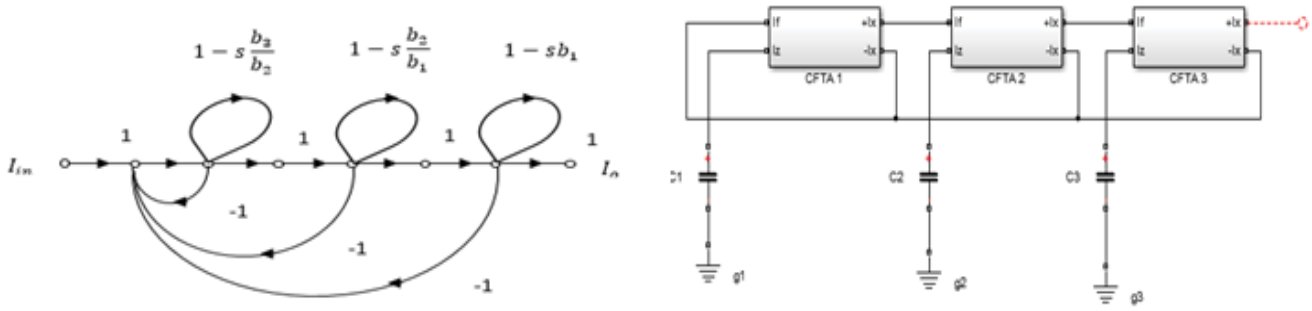

Figure 9. Third-order low-pass transfer function of equation (4): (a): signal flow graph representation; (b): circuit realization.

Consider for Third-order all-pole low pass Butterworth current transfer function. The corresponding set of equations are:

$I_1=I_{in}-I_2-I_4-I_6$

$$I_2 = I_1 - (1 - s^3 b_3 / b_2) I_2 \Rightarrow I_2 s^3 b_3 / b_2 = I_1$$

$I_3=I_2$

$$I_4 = I_3 - (1 - s^2 b_2 / b_1) I_4 \Rightarrow I_4 s^2 b_2 / b_1 = I_3$$

$I_5=I_4$

$I_6=I_5-(1-sb_1)\, I_6 \Rightarrow I_6\, sb_1=I_5$

$I_{out}=I_6$

And I_{in} represents a source node, I_{out} a sink node.

The third-order low-pass transfer function is considered. Generally, the current transfer function of the normalized third-order Butterworth low-pass filter is defined as:

$$\frac{I_o(s)}{I_{in}(s)} = \frac{1}{b_3 s^3 + b_2 s^2 + b_1 s + 1} = \frac{1}{s^3 + 2s^2 + 2s + 1} \quad (4)$$

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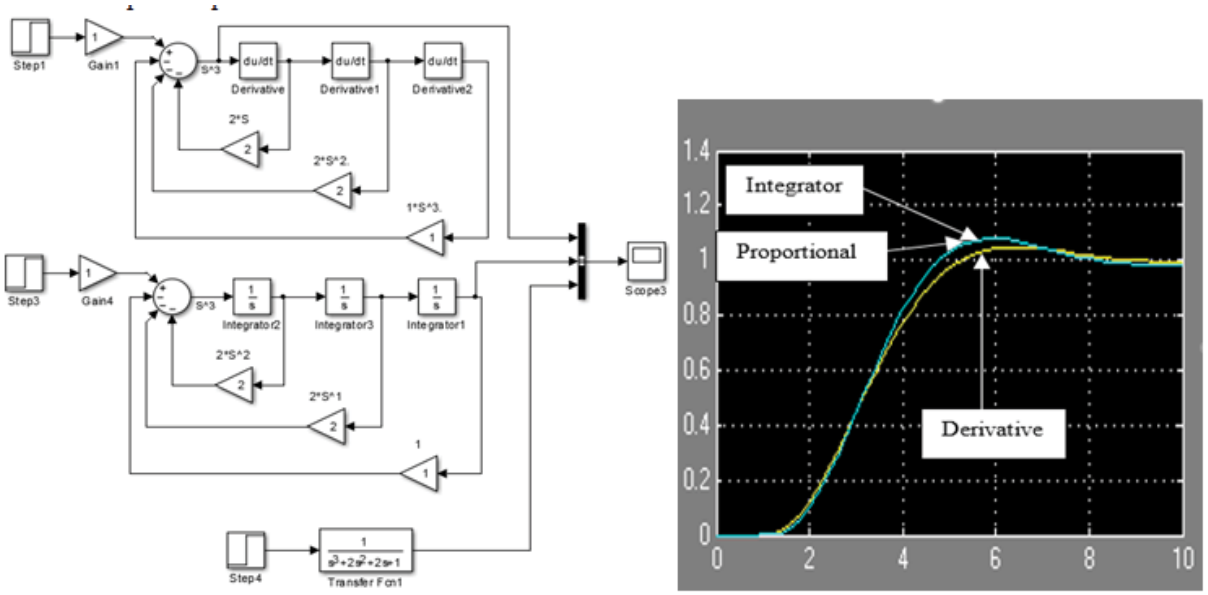

Figure 10. The state-space representation of the transfer function.

Third Order Low Pass Filter of Course Simulink

CDTA-based circuit realization

In this case, the design equations of the circuit are found as:

$$\frac{b_3}{b_2}=\frac{c_1}{g_{m1}}=\frac{1}{2},\ \frac{b_2}{b_1}=\frac{c_2}{g_{m2}}=1,\ b_1=\frac{c_3}{g_{m3}}=2 \text{ and } b_o=1 \quad (5)$$

Thus, the normalized component values are obtained as $C_1=C_2=C_3=1F$, $g_{m1}=\frac{2A}{V}$, $g_{m2}=\frac{1A}{V}$, $g_{m3}=\frac{1A}{V}$. Routine circuit analysis of **Figure 6b** yields the current transfer function as follows:

$$\frac{I_o(s)}{I_{in}(s)}=\frac{\frac{g_{m1}g_{m2}g_{m3}}{C_1C_2C_3}}{s^3+\left(\frac{g_{m1}}{C_1}\right)s^2+\left(\frac{g_{m1}g_{m2}}{C_1C_2}\right)s+\left(\frac{g_{m1}g_{m2}g_{m3}}{C_1C_2C_3}\right)} \quad (6)$$

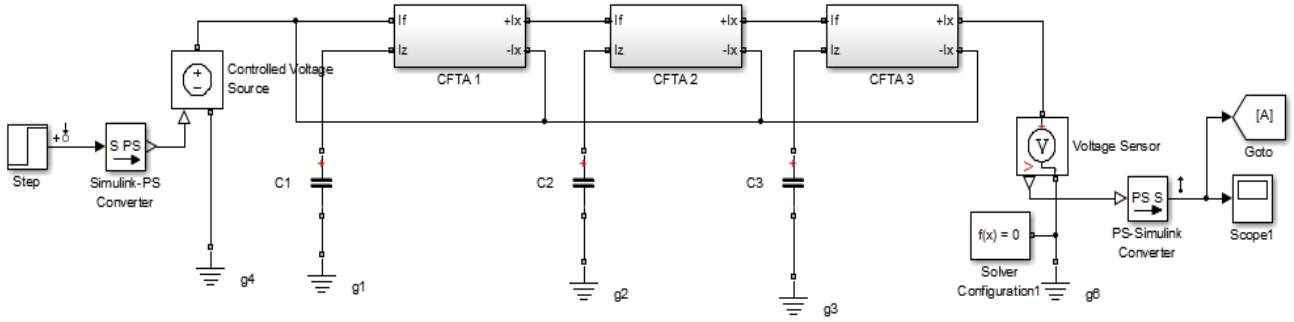

Figure 11. Model for third-order low-pass transfer function.

The active and passive sensitivities of the natural angular frequency (w) and quality factor (Q) are calculated using relations given in Soderstrand MA [18]. The results of active and passive sensitivity analysis of various parameters for the proposed filter are given in **Table 2**. It is clearly seen from **Table 2** that all the sensitivities are low and within unity in magnitude. Thus, all the sensitivities are small.

Table 2. Sensitivities for the circuit parameters in **Figure 9**.

	gm1	gm2	gm3	c1	c2	c3
b_0	1	1	1	-1	-1	-1
b_1	1	1	0	-1	-1	0

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b_2	1	0	0	-1	0	0
W_0	0	1	0	0	-1	0
Q	-1	0	1	1	0	-1

Fourth-Order Butterworth Lowpass Filter

Fourth-order all-pole low pass Butterworth current transfer function. It can easily show that this transfer function can be represented by the signal flow graph shown in **Figure 12a** and the corresponding circuit realization of this graph is thus shown in **Figure 12b.**

Consider for fourth-order all-pole low pass Butterworth current transfer function. The corresponding set of equations are:

$I_1=I_{in}-I_2-I_4-I_6-I_8$

$$I_2 = I_1 - (\frac{1-s^4 b_4}{b_3})I_2 \Rightarrow I_2 \frac{s^4 b_4}{b_3} = I_1$$

$I_3=I_2$

$$I_4 = I_3 - (\frac{1-s^3 b_3}{b_2})I_4 \Rightarrow I_4 \frac{s^3 b_3}{b_2} = I_3$$

$I_5=I_4$

$$I_6 = I_5 - (\frac{1-s^2 b_2}{b_1})I_6 \Rightarrow I_6 \frac{s^2 b_2}{b_1} = I_5$$

$I_7=I_6$

$I_8=I_7-(1-s_1)\, I_8 \Rightarrow I_8\, sb_1=I_7$ (7)

$I_{out}=I_8$

And $I_{(in)}$ represents a source node, I_{out} a sink node.

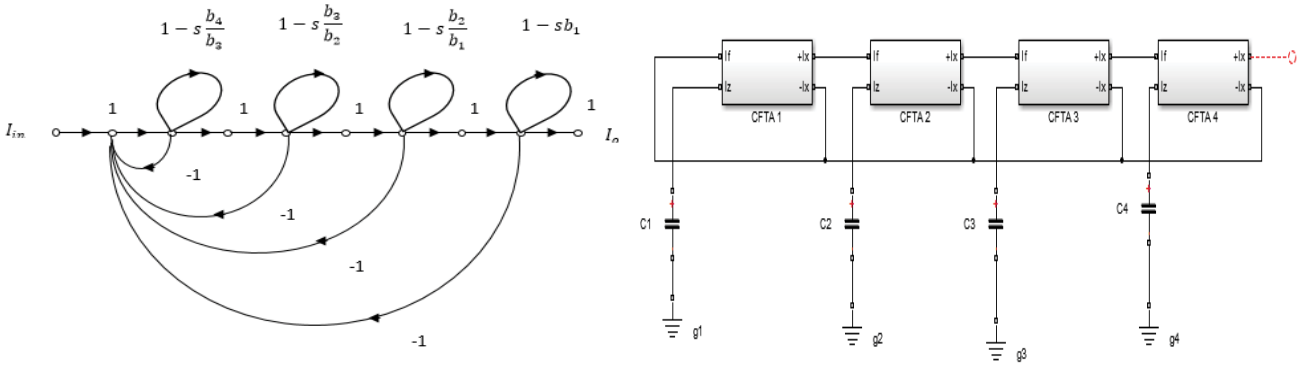

Figure 12. Fourth-order low-pass transfer function of equation (6), (a): signal flow graph representation; (b): circuit realization.

The fourth-order low-pass transfer function is considered. Generally, the current transfer function of the normalized fourth-order Butterworth low-pass filter is defined as

$$\frac{I_o(s)}{I_{in}(s)} = \frac{1}{b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s + 1} = \frac{1}{s^4 + 2s^3 + 3s^2 + 2s + 1} \quad (8)$$

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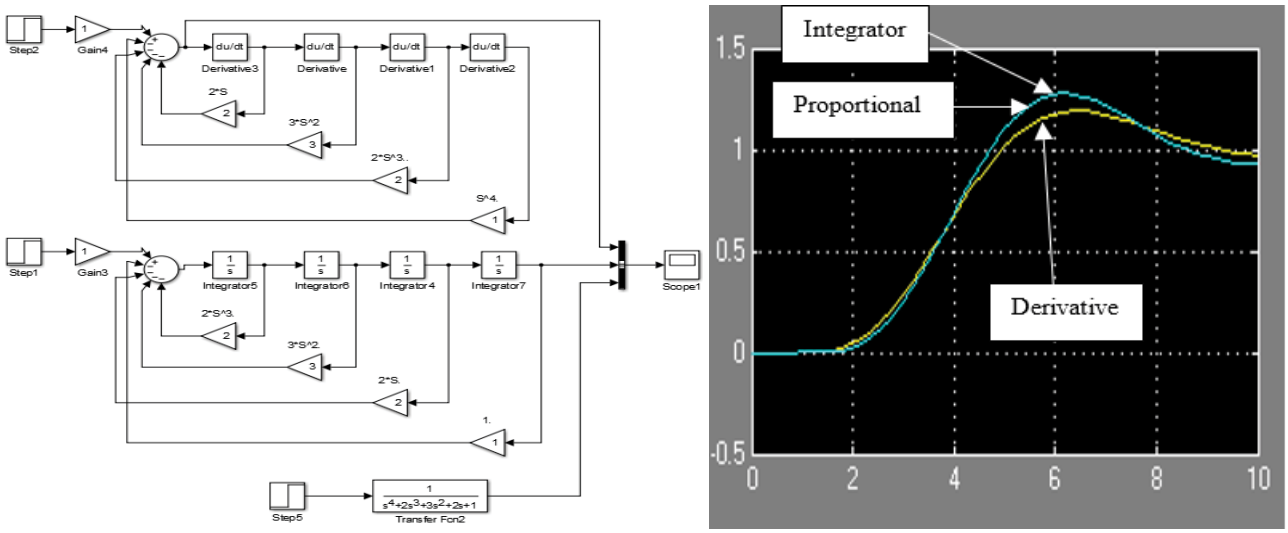

Figure 13. The state-space representation of the transfer function.

Fourth Order Low Pass Filter of Course Simulink

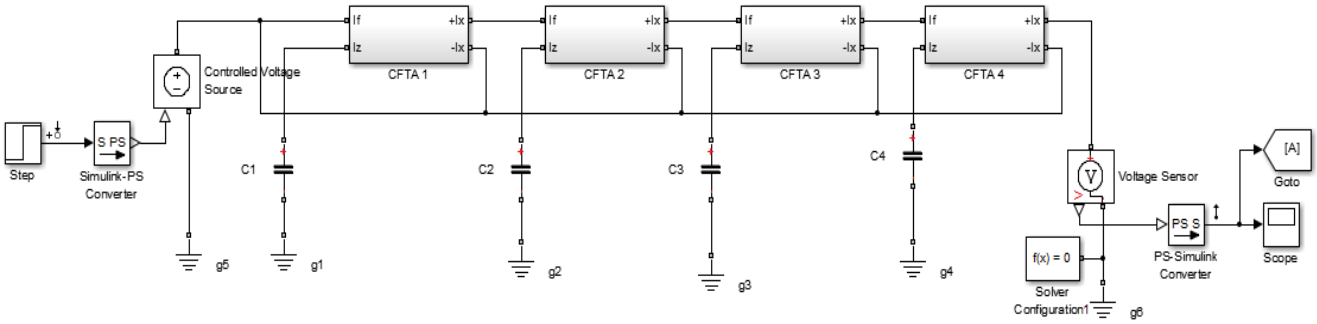

Figure 14. Model for the fourth-order low-pass transfer function.

In this case, the design equations of the circuit are found as:

$$\frac{b_4}{b_3}=\frac{c_1}{g_{m1}}=\frac{1}{2},\frac{b_3}{b_2}=\frac{c_2}{g_{m2}}=\frac{2}{3},\frac{b_2}{b_1}=\frac{c_3}{g_{m3}}=\frac{3}{2},b_o=\frac{C_4}{g_{m4}}=2 \text{ and } b_0=1. \quad (9)$$

thus, the normalized component values are obtained as C1=C2=C3=C4=1F, $g_{m1}=2A/V, g_{m2}=3/2\ A/V,\ g_{m3}=2/3\ A/V$ and $g_{m4}=1/2\ A/V$. Routine circuit analysis of **Figure 8b** yields the current transfer function as follows:

$$\frac{I_o(s)}{I_{in}(s)}=\frac{\frac{g_{m1}g_{m2}g_{m3}g_4}{C_1C_2C_3C_4}}{s^4+\left(\frac{g_{m1}}{C_1}\right)s^3+\left(\frac{g_{m1}g_{m2}}{C_1C_2}\right)s^2+\left(\frac{g_{m1}g_{m2}g_{m3}}{C_1C_2C_3}\right)s+\left(\frac{g_{m1}g_{m2}g_{m3}g_{m4}}{C_1C_2C_3C_4}\right)} \quad (10)$$

Fifth-Order Butterworth Lowpass Filter

Fifth-order all-pole low pass Butterworth current transfer function. It can easily show that this transfer function can be represented by the signal flow graph shown in **Figure 15a**, and the corresponding circuit realization of this graph is thus shown in **Figure 15b**.

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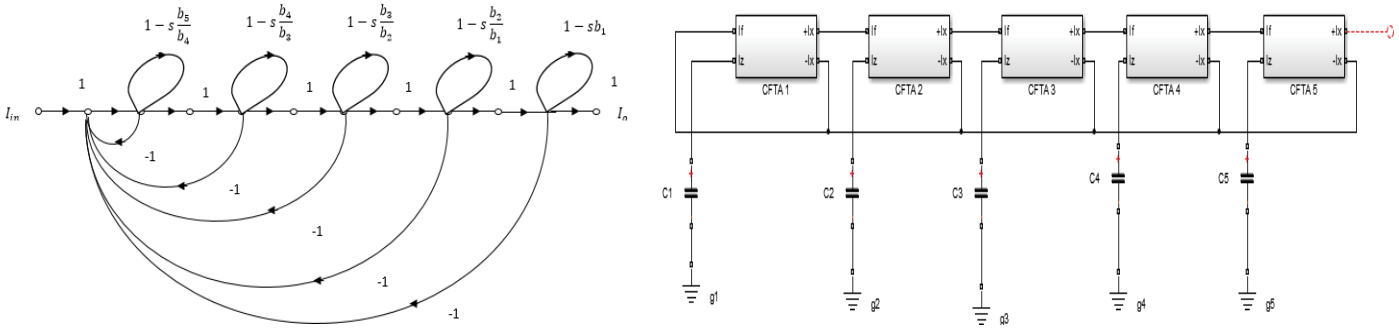

Figure 15. Fifth-order low-pass transfer function of equation (7), (a): signal flow graph representation; (b): circuit realization.

Consider for fifth-order all-pole low pass Butterworth current transfer function. The corresponding set of equations are:

$I_1=I_{in}-I_2-I_4-I_6-I_8-I_{10}$

$$I_2 = I_1 - (\frac{1-s^5 b_5}{b_4})I_2 \Rightarrow I_2 \frac{s^4 b_4}{b_3} = I_1$$

$I_3=I_2$

$$I_4 = I_3 - (\frac{1-s^4 b_4}{b_3})I_4 \Rightarrow I_4 \frac{s^3 b_3}{b_2} = I_3$$

$I_5=I_4$

$$I_6 = I_5 - (\frac{1-s^3 b_3}{b_2})I_6 \Rightarrow I_6 \frac{s^2 b_2}{b_1} = I_5$$

$I_7=I_6$

$$I_8 = I_7 - (\frac{1-s^2 b_2}{b_1})I_8 \Rightarrow I_8 s b_1 = I_7$$

$I_9=I_7$

$I_{10}=I_9-(1-sb_1)I_{10} \Rightarrow I_{10}\, sb_1=I_9$

$I_{out}=I_{10}$

And $I_{(in)}$ represents a source node, I_{out} a sink node.

The fifth-order low-pass transfer function is considered. Generally, the current transfer function of the normalized fifth-order Butterworth low-pass filter is defined as

$$\frac{I_o(s)}{I_{in}(s)} = \frac{1}{b_5 s^5 + b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s + 1} = \frac{1}{s^5 + 3s^4 + 5s^3 + 5s^2 + 3s + 1} \quad (11)$$

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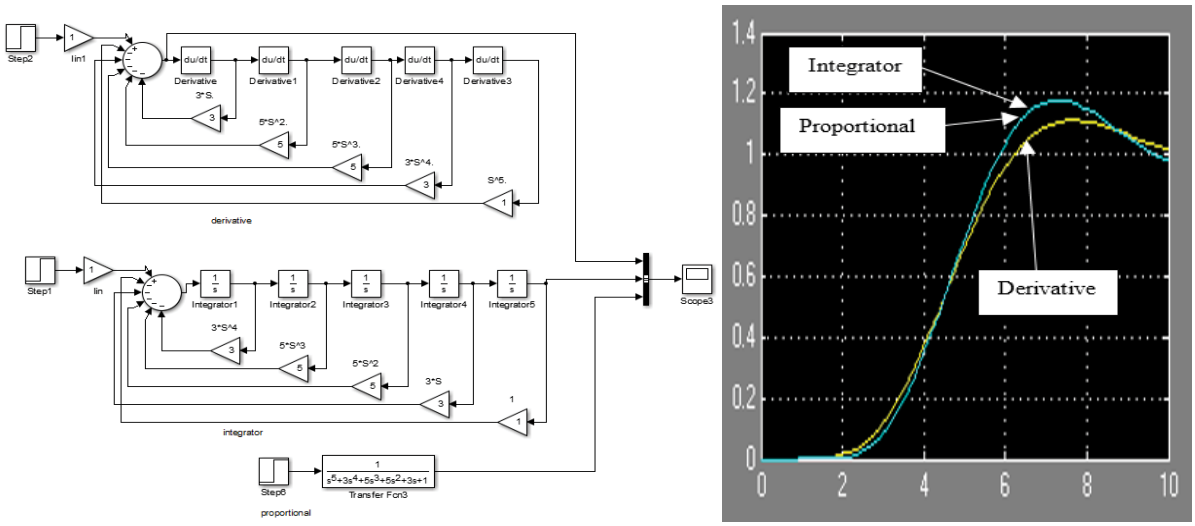

Figure 16. The state-space representation of the transfer function.

Fifth Order Low Pass Filter of Course Simulink

CDTA-based circuit realization

In this case, the design equations of the circuit are found as:

$$g_{m1}=2A/V, g_{m2}=\tfrac{3}{2}A/V,\ g_{m3}=\tfrac{2}{3}A/V, g_{m4}=\tfrac{1}{2}A/V \quad ,b_0=1. \tag{12}$$

thus, the normalized component values are obtained as $C_1=C_2=C_3=C_4=C_5=1F$, $g_{m1}=2A/V, g_{m2}=\tfrac{3}{2}A/V,\ g_{m3}=\tfrac{2}{3}A/V, g_{m4}=\tfrac{1}{2}A/V$ and $g_{m5}=\tfrac{1}{3}A/V$. Routine circuit analysis of **Figure 13b** yields the current transfer function as follows:

$$\frac{I_o(s)}{I_{in}(s)}=\frac{\frac{g_{m1}g_{m2}g_{m3}g_{m4}g_{m5}}{C_1C_2C_3C_4C_5}}{s^5+\left(\frac{g_{m1}}{C_1}\right)s^4+\left(\frac{g_{m1}g_{m2}}{C_1C_2}\right)s^3+\left(\frac{g_{m1}g_{m2}g_{m3}}{C_1C_2C_3}\right)s^2+\left(\frac{g_{m1}g_{m2}g_{m3}g_{m4}}{C_1C_2C_3C_4}\right)s+\left(\frac{g_{m1}g_{m2}g_{m3}g_{m4}g_{m5}}{C_1C_2C_3C_4C_5}\right)} \tag{13}$$

From (10) and (13), the coefficient sensitivities to active and passive components $\left(\left|S^{b_i}_{g_{mi}}\right| and \left|S^{b_i}_{C_i}\right|\right)$ are 1 or 0. Also, the active and passive sensitivities of the natural angular frequency and quality factor $\left(\left|S^{w_o}_{g_{mi},C_i}\right| and \left|S^{Q}_{g_{mi}C_i}\right|\right)$ are calculated and found as 1 or 0 [18]. Thus, all the sensitivities are small.

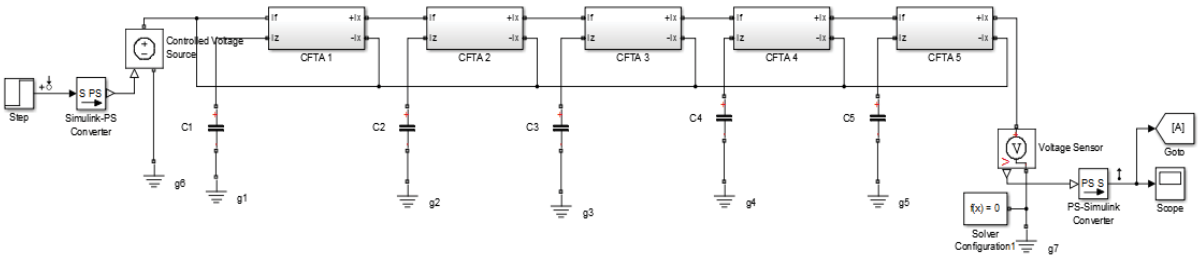

Figure 17. Model for the fifth-order low-pass transfer function.

DESIGN AND SIMULATION RESULTS

The workability of the proposed circuits was tested and verified in MATLAB Simulink using 0.35 µm CMOS process parameters provided by MOSIS (AGILENT) and the Bipolar parameters for NR100N (NPN) and PR100N (PNP) [19] as listed in **Table 3**.

The DC supply voltages and bias currents were respectively selected as: +V=-V=3 V and I_B=100 µA. In this case, the transconductance gain (g_m) of the CFTA is directly proportional to the external bias current I, which is approximately equal to:

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$g_m = \frac{I_o}{2V_T}$ and $V_T \cong 26$ mV at 27 °C.

As an example, the illustrative current-mode third, fourth and fifth order all-pass filter of **Figures 9-17** was designed with ω_0=106 rad/sec. For this purpose, the denormalized component values were chosen as $C1=C_2=C_3=C_4=C_5$=1nF.

First-Order

g_{m1}=2mA/V ($I_{01} \cong$ 104 μA), g_{m2}=1 mA/V ($I_{02} \cong$ 52 μA), and g_{m3}=1/2 mA/V ($I_{03} \cong$ 26 μA).

Second-Order

g_{m1}=2 mA/V ($I_{01} \cong$ 104 μA), g_{m2}=3/2 mA/V ($I_{02} \cong$ 78 μA), and g_{m3}=2/3 mA/V ($I_{03} \cong$ 35 μA),and g_{m4}=1/2 mA/V ($I_{04} \cong$ 26 μA).

Third-Order

g_{m1}=3 mA/V ($I_{01} \cong$ 156 μA), g_{m2}=5/3 mA/V ($I_{02} \cong$ 87 μA), and g_{m3}=1 mA/V ($I_{03} \cong$ 52 μA), g_{m4}=3/5 mA/V ($I_{04} \cong$ 31.2 μA), g_{m5}=1/3 mA/V ($I_{04} \cong$ 17.3 μA)

Table 3. Bipolar and CMOS process parameters.

Transistor	Process Parameters
NR100N	IS=121E-18, BF=137.5, VAF=159.4, IKF=6.974E-3, ISE=36E-16, NE=1.713, BR=0.7258, VAR=10.73, IKR=2.198E-3, RE=1, RB=524.6, RBM=25, RC=50, CJE=0.214E12, VJE=0.5, MJE=0.28, CJC=0.983E-13, VJC=0.5, MJC=0.3, XCJC=0.034, CJS=0.913E-12, VJS=0.64, MJS=0.4, FC=0.5, TF=0.425E-8, TR=0.5E-8, EG=1.206, XTB=1.538, XTI=2.0
PR100N	IS=73.5E-18, BF=110, VAF=51.8, IKF=2.359E-3, ISE=25.1E-16, NE=1.650, BR=0.4745, VAR=9.96, IKR=6.478E-3, RE=3, RB=327, RBM=24.55, RC=50, CJE=0.18E12, VJE=0.5, MJE=0.28, CJC=0.164E-12, VJC=0.8, MJC=0.4, XCJC=0.037, CJS=1.03E-12, VJS=0.55, MJS=0.35, FC=0.5, TF=0.610E-9, TR=0.610E-8, EG=1.206, XTB=1.866, XTI=1.7
nMOS	LEVEL=3, UO=460.5, TOX=1E-8, TPG=1, VTO=0.62, JS=1.8E-6, XJ=0.15E-6, RS=417, RSH=2.73, LD=4E-8, ETA=0, VMAX=130E3, NSUB=1.71E17, PB=0.761 PHI=0.905, THETA=0.129, GAMMA=0.69, KAPPA=0.1, AF=1, WD=1.1E-7, CJ=76.4E-5, MJ=0.357, CJSW=5.68E-10, MJSW=0.302, CGSO=1.38E-10, CGDO=1.38E-10, CGBO=3.45E-10, KF=3.07E-28, DELTA=0.42, NFS=1.2E11
pMOS	LEVEL=3, UO=100, TOX=1E-8, TPG=1, VTO=-0.58, JS=0.38E-6, XJ=0.1E-6, RS=886, RSH=1.81, LD=3E-8, ETA=0, VMAX=113E3, NSUB=2.08E17, PB=0.911, PHI=0.905, THETA=0.12, GAMMA=0.76, KAPPA=2, AF=1, WD=1.4E-7, CJ=85E-5, MJ=0.429, CJSW=4.67E-10, MJSW=0.631, CGSO=1.38E-10, CGDO=1.38E-10, CGBO=3.45E-10, KF=1.08E-29, DELTA=0.81, NFS=0.52E11

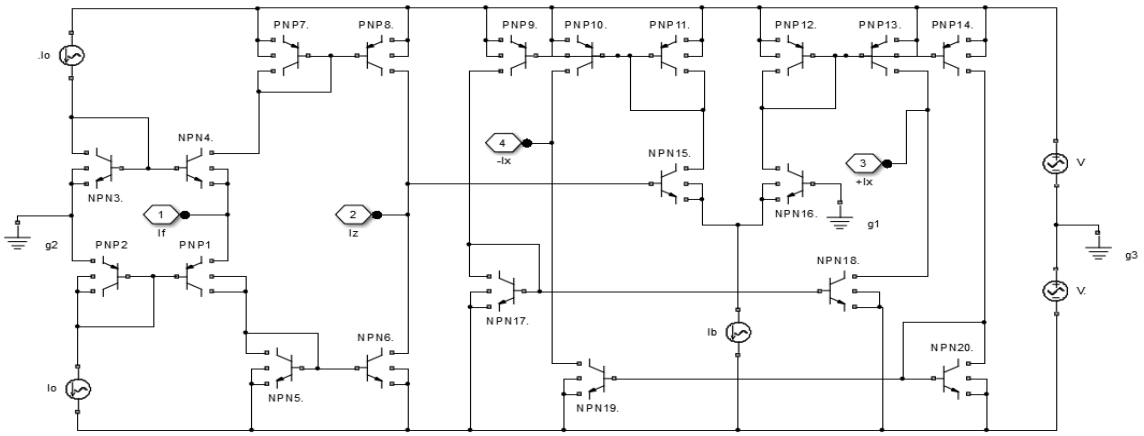

Figure 18. Bipolar implementation of the CFTA used for simulations.

The power supply rail voltages and bias currents were respectively selected as: ± V= 1.85 V and I_B=400 μA. In this case, the transconductance gain (g_m) of the CFTA is CMOS based 1th CFTA (i=1,2,3), and can be controlled through the biasing current IB which can also be written by $g_{mi} = \sqrt{\beta_o I_o}$ where $\beta_o = \mu_o C_{ox}\left(\frac{W}{L}\right)$ is the process parameter, μ_0 is the free electron mobility in the channel, C_{OX} is the gate oxide capacitance per unit area, W and L are the channel width and length respectively. For the parameters $\beta_i = \mu_o C_{ox}\left(\frac{W}{L}\right)_{1,2} = \mu_o C_{ox}\left(\frac{W}{L}\right)_{3,4}$ and $\beta_B = \mu_o C_{ox}\left(\frac{W}{L}\right)_{18,19}$ However, I_0 and I_B are input bias current to control g_{mi} and g_m, and can be respectively written as $g_{mi} = \sqrt{\beta_o I_o}$ and $g_m = \sqrt{2\beta_B I_B}$ **(Figures 18 and 19)**.

For 0.5 μm CMOS process used in this case, $KP=(\mu_o C_{OX})_{pMOS}$ and $KP=(\mu_o C_{OX})_{nMOS}$ were given. Therefore, the aspect ratios of MOS Transistors for CFTA and the dimensions of MOS transistors were used as specified in **Table 4**.

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Table 4. Transistor dimensions of CMOS implemented CFTA.

NMOS transistor	Dimensions W (μm)/L(μm)	PMOS transistor	Dimensions W (μm)/L(μm)
M3, M4, M7, M8	1.0/1.0	M1, M2, M5, M6	3.1/1.0
M10, M12, M13, M14, M15, M20	1.0/1.0	M9, M11, M16, M17, M18, M19	3.1/1.0

As an example, the illustrative current-mode third, fourth and fifth-order all-pass filter of **Figures 9-17** were designed with ω_0=106 rad/sec. For this purpose, the denormalized component values were chosen as

Fourth-Order

g_{m1}=147.3 μA/V ($I_{01} \cong$ 104 μA), g_{m2}=104.6 μA/V ($I_{02} \cong$ 52 μA), and g_{m3}=73.65 μA/V ($I_{03} \cong$ 26 μA). C_1=73.65pF, C_2=104.6 pF, and C_3=147.3 pF.

Fifth-Order

g_{m1}=147.3 μA/V ($I_{01} \cong$ 104 μA), g_{m2}=127.6 μA/V ($I_{02} \cong$ 78 μA), and g_{m3}=85.45 μA/V ($I_{03} \cong$ 35μA),and g_{m4}=73.65 μA/V ($I_{04} \cong$ 26μA), C_1=73.65 pF, C_2=85.07 pF, C_3=128.72 pF, and C_4=147.3 pF.

Sixth-Order

g_{m1}=180.41 μA/V ($I_{01} \cong$ 156 μA), g_{m2}=134.7 μA/V ($I_{02} \cong$ 87 μA), and g_{m3}=104.16 μA/V ($I_{03} \cong$ 52 μA), g_{m4}=80.7 μA/V ($I_{04} \cong$ 31.2μA), g_{m5}=60.18 μA/V ($I_{04} \cong$ 17.3μA), C_1=36.14 pF, C_2=80.8pF, C_3=104.16 pF, C_4=134.5 pF and C_5=180.23 pF.

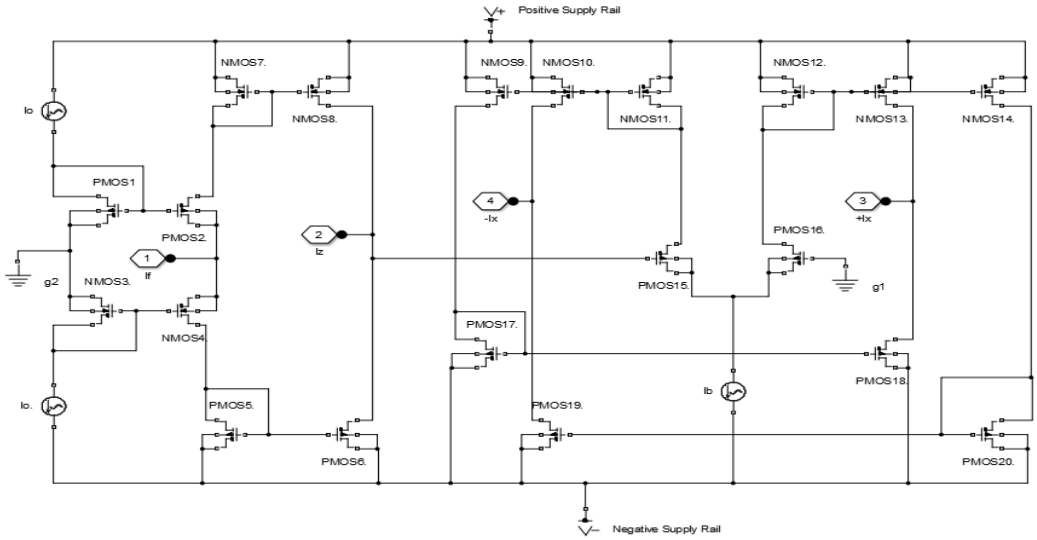

Figure 19. CMOS implementation of the CFTA used for simulations.

The simulated third, fourth and fifth-order all-pole low pass circuits with the theoretical values are shown in **Figure 20**, which is obtained by applying a sinusoidal input of bias currents at 159 kHz.

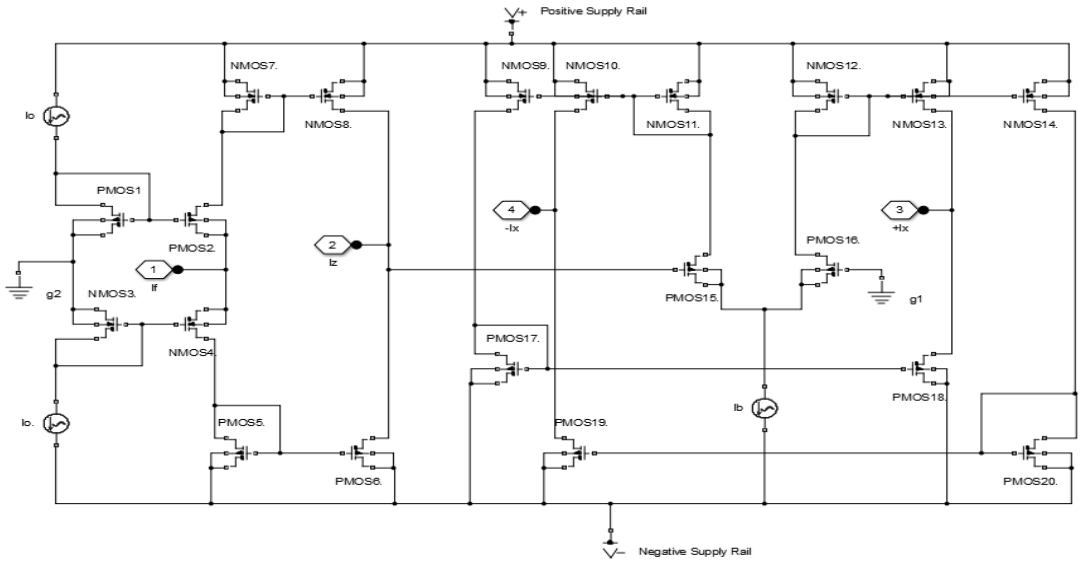

Figure 20. Simulated third, fourth and fifth-order all-pole low pass circuits.

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Ideal gain and phase responses of the third, fourth and fifth-order all-pole low pass filter responses compared with the theoretical values are shown in **Figure 21**.

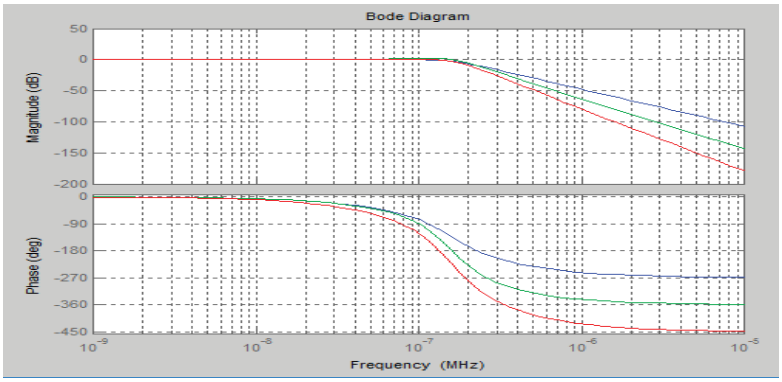

Figure 21. Gain and phase responses of the third, fourth and fifth-order all-pole low pass filter.

The time-domain analysis of third-order all-pole low pass filter is also shown in **Figure 22**, which is obtained by applying a sinusoidal input of 150 µA peak to peak at 0.159 Hz.

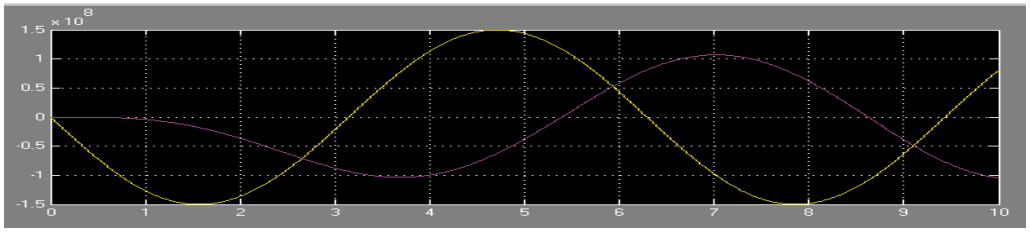

Figure 22. Time-domain response of proposed third-order all-pole low pass filter with respect to sinusoidal current output/input signal.

The time-domain analysis of the fourth-order all-pole low pass filter is also shown in **Figure 23**, which is obtained by applying a sinusoidal input of 40 µA peak at 0.159 Hz.

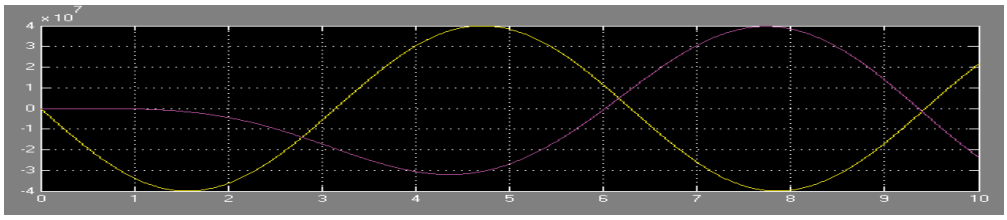

Figure 23. time domain response of proposed fourth-order all-pole low pass filter with respect to sinusoidal current output/input signal.

The time-domain analysis of the fifth order all-pole low pass filter is also shown in **Figure 24** which is obtained by applying a sinusoidal input of 10 µA peak at 0.159 Hz.

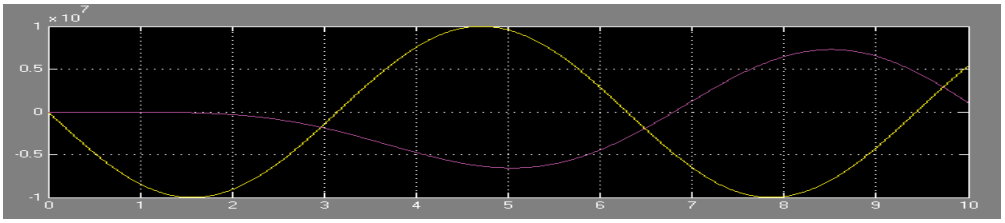

Figure 24. Time-domain response of proposed fifth-order all-pole low pass filter with respect to sinusoidal current output/input signal.

The THDs of the proposed fifth-order all-pole low pass filter can also be verified by applying multi-tones to the filters at the bias current equal to 100 µA at a constant frequency of 159 kHz. From **Figure 25**, it appears that the cut of band tones has been removed and only the in-band tones can be obtained at the output.

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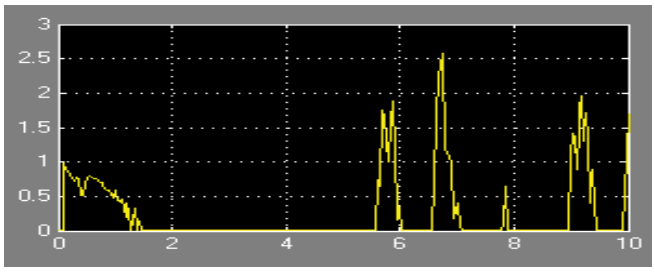

Figure 25. The THDs of the proposed fifth-order all-pole low pass filter.

The comparison between the proposed third-order Butterworth low pass filter, fourth-order Butterworth low pass filter and fifth-order Butterworth low pass filter is expressed in **Table 5**.

Table 5. Fourth-order Butterworth low pass filter and fifth-order Butterworth low pass filter.

Features	Proposed		
	Third-Order Butterworth Low Pass Filter	Fourth-Order Butterworth Low Pass Filter	Fifth-Order Butterworth Low Pass Filter
Number of Active Element		4 CFTA	5 CFTA
Nyumber of Passive Element	$C_1=C_2=C_3$=1nF	$C_1=C_2=C_3$=1nF	$C_1=C_2=C_3$=1nF
tunability of Q and W0	yes	yes	yes
Low active-passive sensitivity	yes	yes	yes
Power Supply Rails(CMOS)	± V=0.75 V	± V=0.75 V	± V=0.75 V
Supply voltage (Bipolar)	± V=3 V	± V=3 V	± V=3 V
Designed pole frequency	159 KHz	159 KHz	159 KHz
Type of dependence on the bias current	non-linear	non-linear	non-linear
Matching condition required	NO	NO	NO
power consumed	NA	NA	NA

CONCLUSION

In this paper, a Signal flow graph to synthesize the general, all-pole low pass current transfer function by an active-C circuit using the SFG representation of any nth-order all-pole low pass circuit requires only n CFTAs and n grounded capacitors. Third-order Butterworth low pass circuit require only three CFTAs and three grounded capacitors, fourth-order Butterworth low pass circuit require only four CFTAs and four grounded capacitors and fifth-order Butterworth low pass circuit require only five CFTAs and five grounded capacitors. The approach is based on drawing a signal flow graph directly from the graph of Active-C filter involving CFTA. It has been shown that the resulting structures are canonical in the number of active components n CFTAs for realizations, making them especially suitable for integration. The circuits also have low sensitivity characteristics and exhibit electronic controllability coefficients via transconductance gains gm of CFTAs. The simulation results from MATLAB Simulink are in excellent agreement with theoretical assumptions. However, a slight deviation may arise due to the parasitic involved. The circuit is operated at a supply voltage of ± 3 V, power supply rails of ± 1.85 V, and power dissipation of 10.6 mW, which are attractive for battery-operated portable electronic gadgets and mobile communication systems. The use of CFTAs as active elements in the filter design, in which there is the availability of high impedance explicit output terminals for proper impedance matching and no external buffers will be needed to draw the current-mode responses. High impedance explicit outputs are also suitable for direct cascading to implement higher-order current mode all-pole low pass filters using CFTAs.

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