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Simulation and Analysis of A ZVT and ZCT Interleaved DC-DC Boost Converter

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ABSTRACT—In this paper, an interleaved boost converter with zero-voltage transition and zero-current transition characteristics is proposed. The interleaved approach reduces the ripple of the input current and output voltage. The active snubber cell provides main switch to turn ON with zero-voltage transition (ZVT) and to turn OFF with zero-current transition (ZCT). All semiconductor devices operate with soft switching. There is no additional voltage stress across the main and auxiliary components. The proposed converter has simple structure, minimum number of components, and ease of control. The operating principle and detailed steady-state analysis of the converter are given. The proposed converter is simulated using MATLAB/SIMULINK

KEYWORDS— soft switching, zero-voltage transition (ZVT), zero-current transition (ZCT), interleaved boost converter.

I. INTRODUCTION

An Interleaved boost converter usually combines more than two conventional topologies and the current in the element of the interleaved boost converter is half of the conventional topology in the same power condition. Besides, the input current ripple and output voltage ripple of the interleaved boost converter are lower than those of the conventional topologies.

The single boost converter can use the zero-voltage transition (ZVT) and/or zero-current transition (ZCT) to reduce the switching loss at the high frequency switching [1]-[9]. High-Frequency PWM dc–dc converters have been widely used in power factor correction, battery charging, and renewable energy applications due to their high power density, fast response, and control simplicity. To achieve high-power density and smaller converter size, it is required to operate converters at high switching frequencies. However, they are considered for the single topology. Many soft-switching techniques are introduced to the interleaved boost converter. In [10] the Zero-current-switching performance is used to reduce the switching losses by using coupled inductors in the interleaved boost converter.The cost of the converter is increased due to the usage of the coupled inductors.

In [11], [12], [13] zero voltage switching (ZVS) and zero current switching (ZCS) characteristics is achieved for the main switches of the interleaved boost converter. The ZVS and ZCS can operate only at variable frequency control to regulate the output. This is undesirable since it complicates the control circuit and generates unwanted EMI harmonics especially under wide load variations.
In some papers [14] only ZVT characteristics is alone achieved for the main switches of the interleaved boost converter.

This paper proposes an interleaved boost converter with an active Snubber cell is proposed. The active snubber cell provides both characteristics of zero-voltage transition during turn ON of the switch and zero-current transition during turn OFF of the switch. The proposed converter is the parallel of two boost converters with their driving signals stagger 180 and this makes the operation assumed symmetrical. The converter has simple structure, minimum number of components, and ease of control.

II. OPERATION MODES AND ANALYSIS

A. Definitions and Assumptions

Interleaved ZVT-ZCT PWM boost converter circuit is shown in Fig.1. In this circuit, input voltage source isV_i, output voltage isV_o,L_F,L_{F1}, is main inductor, $C_F$is output filter capacitor, and D_F,D_{F1} is main diode. The

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main switch S_1, S_3 consist of a main transistor T_1, T_3 and its body diode D_1, D_3. The snubber circuit shown with dashed line is formed by snubber inductor L_S, L_{S1} a snubber capacitor C_S, $C_{S1}$and auxiliary switch S_2, S_4 consist of a transistor T_2, T_4 and its body diode D_2, D_4. The capacitor C_r, $C_{r1}$is assumed to be the sum of the parasitic capacitor of T_1, T_3 and the other parasitic capacitors incorporating it. In the proposed converter, it is not required to use an additional C_r capacitor.

B. Operation Modes of the converter

In Fig. 2(a)-(k), the equivalent circuit diagram of the operation modes are given respectively. The pulse waveforms for switches are shown in Fig. 3. The detailed analysis of the proposed circuit is presented below.

Mode 1[t_0 < t <t_1: Fig.2 (a)]: At the beginning of this mode the main diode D_F is in the ON state and the input current I_i flows through the main diode. The main transistor T_1 and auxiliary transistor T_2 are in OFF state. The initial voltage of the C_S determines the soft-switching range of the circuit. At t=t_0, a resonance starts between snubber inductance L_S and snubber capacitor C_S. Due to the resonance T_2 current rises and D_F current falls. The rise rate of current is limited by the snubber inductance L_S connected serially to the auxiliary switch so that the turn ON of the auxiliary switch is provided with ZCS for this interval, the following equations can be written:

$$i_{LS} = (V_0 - V_{CS0}) \frac{\sin w_s(t-t_0)}{L_s w_s} \quad (1)$$

$$V_{cs} = V_0 - (V_0 - V_{cs0}) \cos w_s(t - t_0) \quad (2)$$

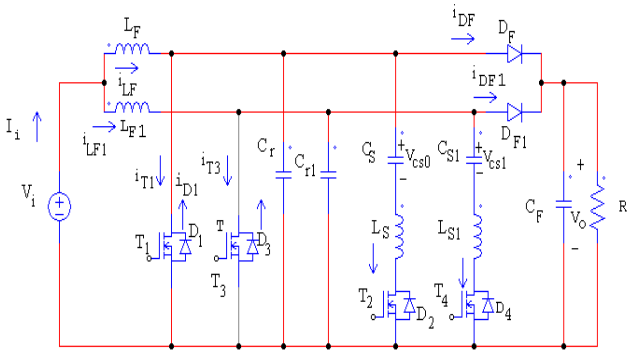

Fig.1 Circuit scheme of the proposed interleaved ZVT-ZCT boost converter.

In these equations

$$w_s = \sqrt{\frac{1}{L_s C_s}} \quad (3)$$

At t=t_1, V_{cs} is charged to V_{cs1}, i_{T2} reaches I_i and i_{DF} falls to zero. When i_{DF} reaches $-I_{rr}$, D_F is turned OFF and this stage finishes. D_F is turned OFF with nearly ZCS and ZVS due to L_S and C_r. At the end of this mode

$$i_{LS} = i_{T2} = I_i + I_{rr} \quad (4)$$

$$V_{cs} = V_{cs1} \quad (5)$$

can be written.

Mode 2 [t_1 < t< t_2: Fig. 2(b)]: Atthe beginning of this modethe auxiliary transistor T_2 is in the ON state and conducts the sum of the input current I_i and the reverse recovery current of D_F. A resonance between parasitic capacitor C_r, L_S, C_S starts. At t=t_2, V_{cr}=0, diode D_1 is turned ON with ZVS. The capacitor C_r is assumed the sum of the parasitic capacitor of T_1 and the other parasitic capacitors incorporating it. At the end of this mode,

$$i_{LS} = i_{T2} = i_{LS2} \quad (6)$$

$$V_{cs} = V_{cs2} \quad (7)$$

are valid.

Mode 3[t_2< t < t_3 : Fig. 2(c)]: At the beginning of this mode the resonant which is between the snubber inductance L_S and snubber capacitor C_S continues and diode D_1 is turned ON and conducts the excess of snubber inductance L_S current from the input current. When control signal is applied to T_1, D_1 is in the ON state in order to provide ZVT turn ON of T_1. At t=t_3, this stage ends when the snubber inductance L_S current falls to input current and D_1 is turned OFF under ZCS. At the end of this mode

$$i_{LS} = i_{T2} = i_{LS3} = I_i \quad (8)$$

$$V_{cs} = V_{cs3} \quad (9)$$

are valid.

Mode 4 [t_3<t <t_4: Fig. 2(d)]: At the beginning of this mode, the main transistor is turned ON with ZVT and its current start to rise. The resonant between snubber

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inductance L_S and snubber capacitor C_S continues. For this mode the following equation are derived:

$$i_{LS} = I_i \cos w_s\,(t - t_3) - \frac{V_{cs4}}{w_s L_s} \sin w_s\,(t - t_3) \quad (10)$$

$$V_{cs} = V_{cs4} \cos w_s(t - t_3) + L_s w_s I_i \sin w_s\,(t - t_3) (11)$$

At t=t_4, the current in the main transistor reaches to the input current level and i_{LS} becomes zero hence the current through the auxiliary transistor reaches zero and T_2 is turned OFF. At the end of this mode,

$$i_{LS} = i_{T2} = I_{LS4} = 0 \ (12)$$

$$V_{cs} = V_{cs4} \ (13)$$

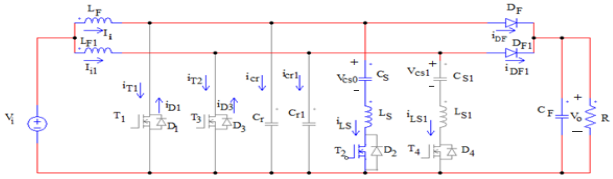
are valid.

Mode 5 [$t_4 < t < t_5$: Fig. 2(e)]: In this mode the diode D_2 is turned ON with ZCS and its current starts to rise. The resonant between snubber inductance and snubber capacitance continues. The current through snubber inductance i_{Ls} becomes negative, so the current through the main transistor is higher than the input current in this mode. The equation is expressed as follows:

$$i_{LS} = -\frac{V_{cs4}}{w_s L_s} \sin w_s\,(t - t_4) \ (14)$$

$$V_{cs} = V_{cs4} \cos w_s\,(t - t_4) \ (15)$$

At t=t_5,the main transistor current decrease to the input current level and i_{LS} becomes zero. i_{D2} becomes zero and it is turned OFF under ZCS. At the end of this mode,



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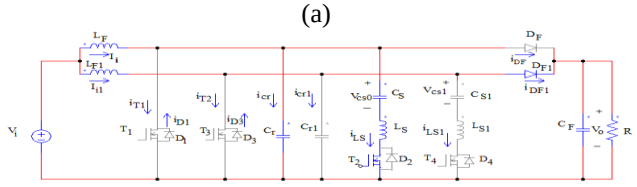

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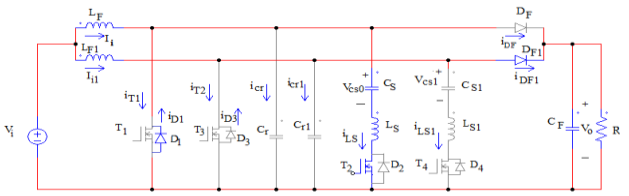

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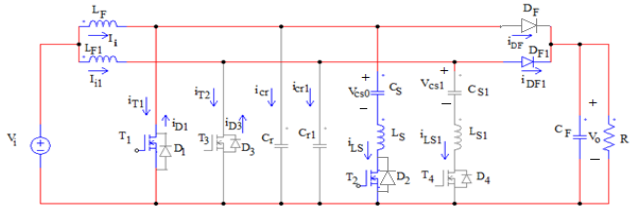

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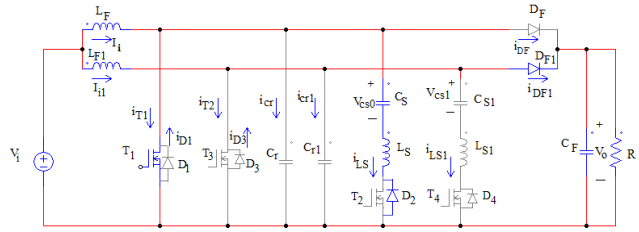

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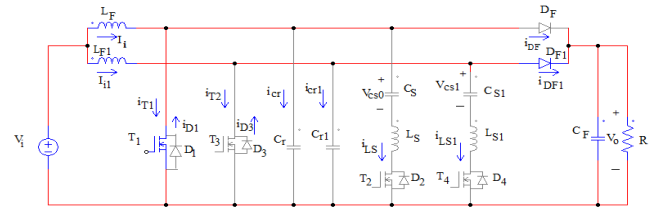

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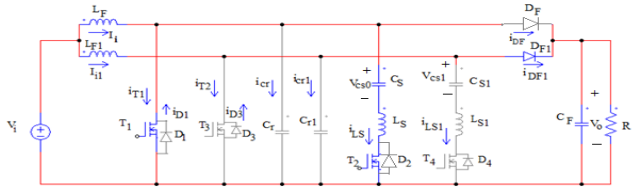
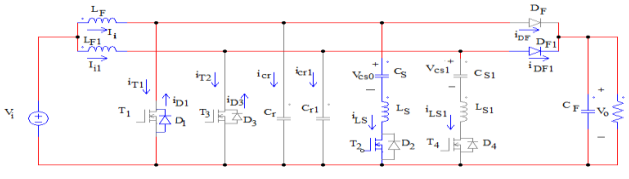


(g)



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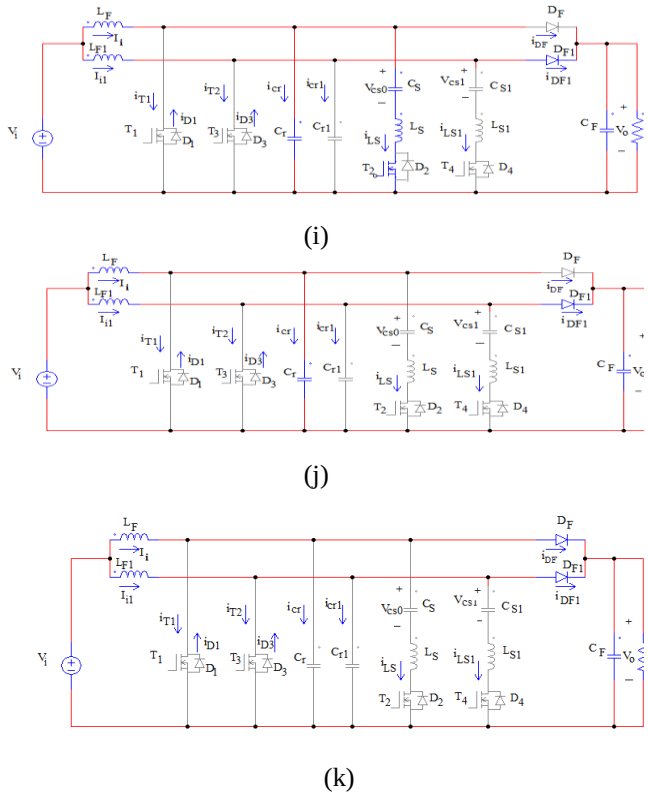

(i)

(j)

(k)

Fig. 2. Equivalent circuit schemes of the operation modes in the proposed novel ZVT-ZCT-PWM boost converter. (a) $t_0 < t < t_1$. (b) $t_1 < t < t_2$. (c) $t_2 < t < t_3$. (d) $t_3 < t < t_4$. (e) $t_4 < t < t_5$(f) $t_5 < t < t_6$. (g) $t_6 < t < t_7$. (h) $t_7 < t < t_8$. (i) $t_8 < t < t_9$. (j) $t_9 < t < t_{10}$. (k) $t_{10} < t < t_{11} = t_0$.

$$i_{LS} = i_{T2} = I_{LS5} = 0 \quad (16)$$

$$V_{cs} = V_{cs5} \quad (17)$$

are valid.

Mode 6 [$t_5 < t < t_6$: Fig. 2(f)]: In this mode main transistor T_1 conducts the input current I_i and snubber circuit is not active. This mode is the ON state of the conventional boost converter.

$$I_{T1} = I_i \quad (18)$$

are valid.

Mode 7 [t6 <t <t7: Fig. 2(g)]: In this mode the control signal is applied to auxiliary transistor T_2, a new resonance between snubber inductance L_S and snubber capacitor C_S. starts through C_S-L_S-T_2-T_1. The equations can be expressed as follows,

$$i_{LS} = -\frac{V_{cs5}}{w_s L_s} \sin w_s (t - t_5) \quad (19)$$

$$V_{cs} = V_{cs5} \cos w_s (t - t_5) \quad (20)$$

The auxiliary transistor T_2 is turned ON with ZCS due to the snubber inductance L_S. The main transistor T_1 current falls with the rise in snubber inductance current.At $t=t_7$, when the current of T_2 reaches to the input current level, the main transistor current becomes zero and this mode finishes.At the end of this mode,

$$i_{LS} = i_{T2} = I_{LS7} = I_i \quad (21)$$

$$V_{cs} = V_{cs7} \quad (22)$$

are valid

Mode 8 [$t_7 < t < t_8$: Fig. 2(h)]: At the beginning of this mode, D_1 is turned ON with ZCS. If T_1 turned OFF when D_1 is ON, T1 turns OFF with ZVS and ZCS. D_1 conducts the excess of i_{LS} from the input current. The resonance between L_S and C_S continues. At=t_8, i_{D1} reaches $-I_{rr}$ and turns OFF, and this stage ends. At the end of this mode

$$i_{LS} = i_{T2} = I_{LS8} = I_i - I_{rr} \quad (23)$$

$$V_{cs} = V_{cs8} = V_{cs0} \quad (24)$$

are valid.

Mode 9 [t8 <t <t9: Fig. 2(i)]: In the beginning of this mode, a resonance between parasitic capacitor C_r, snubber inductor L_S and snubber capacitor C_S starts. At $t=t_9$, i_{LS} falls to zero and the capacitor C_r is charged from zero to V_{cs8} with this resonance. The auxiliary transistor T_2 is turned OFF with ZCS. At the end of this mode

$$i_{LS} = i_{T2} = I_{LS9} = 0 \quad (25)$$

$$V_{cs} = V_{cs9} = V_{cs0} \quad (26)$$

are valid.

Mode 10 [$t_9 < t < t_{10}$: Fig. 2(j)]: In this mode C_r is charged linearly under the input current. At instant $t_{10}$$C_r$ voltage reaches the output voltage V_o, and the main diode D_F is turned ON with ZVS.

Mode 11 [$t_{10} < t < t_{11}$: Fig. 2(k)]: This mode is the OFF state of the conventional boost converter. During this mode, the main diode D_F continues conducting the input

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current I_i and the snubber circuit is not active. For this mode

$$i_{DF} = I_i \qquad (27)$$

can be written.

*Mode 12-22:*since two cells of the converter are identical and operating with the same frequency and duty cycles and there is only 180^0 phase shift between these two cells, the circuit behavior during operation modes of 11-22 is similar to that of during modes of 1–11. The circuit analysis of the converter during the last eleven modes is similar to that of the first eleven modes and can be Achieved by replacing T_1, T_2, D_1, D_2, D_F, L_F, C_r, L_S, C_S,V_{cs0} with T_3, T_4, D_3, D_4, D_{F1}, L_{F1}, C_{r1}, L_{S1}, C_{S1},V_{cs1} respectively.

III DESIGN PROCEDURE

The design procedure for the proposed interleaved ZVT-ZCT boost converter is presented in this section.

1. Operating Requirements:

Output power Pout: 1KW
Input voltage V_{in}: 200V DC
Switching frequency (f_{sw}): 100 KHZ
Output voltage (V_o): 400V

2. Input and Output Parameters:

The relationship between the duty cycle and the Output/input ratio for interleaved boost converter is

$$\frac{V_o}{V_{in}} = \frac{1}{1-D} \qquad (28)$$

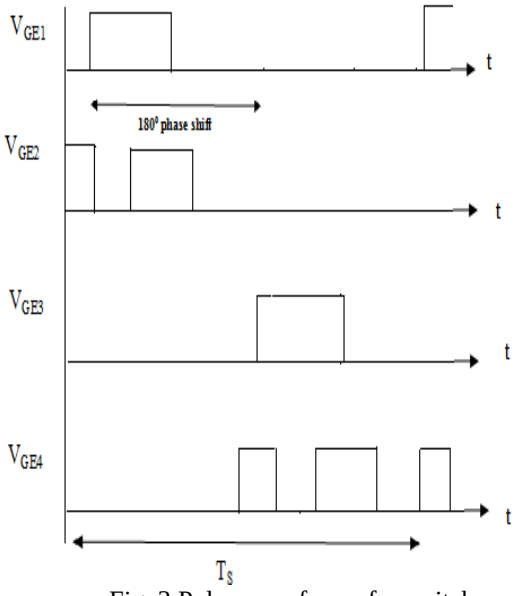

Fig. 3 Pulse waveforms for switches

3. Inductor Current Ripple Peak-To-Peak Amplitude:

The inductor current ripple peak-peak amplitude is given by

$$\Delta I_{l1l2} = \frac{V_{in}\,D}{f_{sw}\,L} \qquad (29)$$

Where f_{sw} is the switching frequency, D is the duty cycle, V_{in} is the input Voltage and L is the inductance.

4. Output Voltage Ripple:

Since the load and output capacitor are supplied through two diodes D_F and D_{F1}, the frequency of the output ripple current is twice the switching frequency. This decreases the output ripple voltageΔV_o. The output capacitor is determined as,

$$C = \frac{V_o D_F}{R\Delta V_o} \qquad (30)$$

5. Selection of Snubber Inductor:

The snubber inductance can be selected to provide the following conditions with reference to [15]. Here, t_{r2} is rise time of the auxiliary switch. V_{cs1} is assumed constant in t_{r2} duration

$$\frac{V_0 - V_{cs1}}{L_s} t_{r2} \leq I_{imax} \qquad (31)$$

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To turn ON auxiliary switch with ZCS, the required Series inductor Ls is calculated as,

$$L_S \geq \frac{400-150}{5} \quad 2 * 10^{-6} \geq 0.1mH (32)$$

The value of L_s is selected as the smallest possible value as 1mH in order to decrease ZCT duration.

6. Selection of Snubber Capacitor:
The snubber capacitor Cs is determined depending on the transient intervals.The sum of the transient intervals isselected to be smaller than 20% oftransient intervals is equal to the resonant period t_R

$$t_R < T_s * \left(\frac{20}{100}\right) (33)$$

$$t_R = 2\pi\sqrt{L_s C_s} (34)$$

The value of Cs is selected as 33μF to obtain appropriate ZVT duration.

IV. SIMULATION RESULTS

The computer simulation of proposed converter is done using MATLAB/SIMULINK and the results are presented. The simulation result of the output voltage and output current are shown in Fig. 4.Soft switching in the auxiliary switch is shown in the Fig.6. Fig.7. Shows the Ripple content in the output voltage.Ripple content in the output voltage is low due to interleavingtechnique. Ripple content in the output voltage is calculated by finding the difference between peak –to–peak voltages. Due to reduce in the ripple content in the output voltage efficiency of the converter is increased.

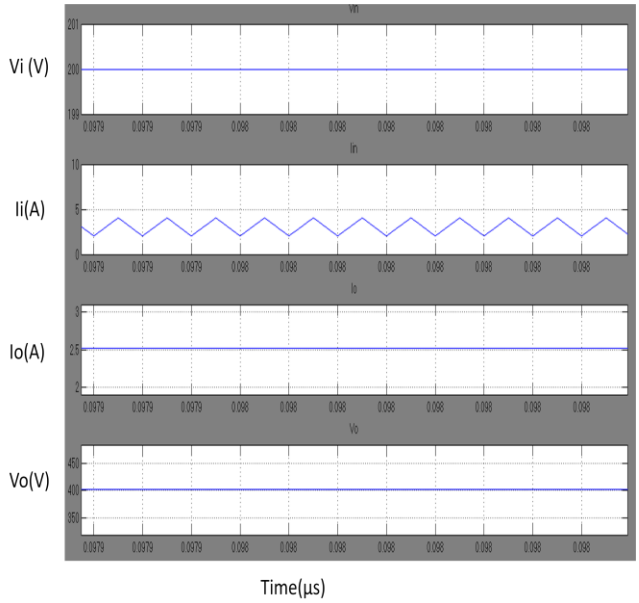

Fig.4 input and output voltage, current waveforms (V_{in}=200V, I_i=5A, V_{out}=400V, I_{out}=2.5A)

Soft switching in the main switch is shown in the Fig.5 Comparisons of the output ripple voltage and THD of conventional ZVT-ZCT boost converter and interleaved ZVT-ZCT boost converter are shown in Table I.

Table I

TYPE	OUTPUT RIPPLE VOLTAGE	THD
ZVT-ZCT Boost Converter	32mV	105.65%
Interleaved ZVT-ZCT Boost Converter	2.8mV	76.02%

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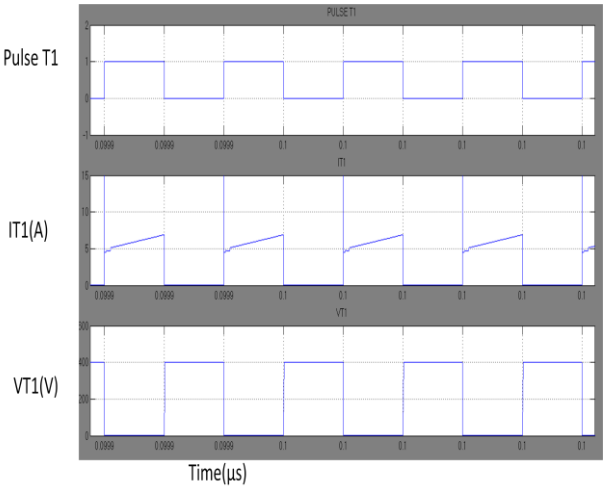

Fig.5 soft switching of the main switch

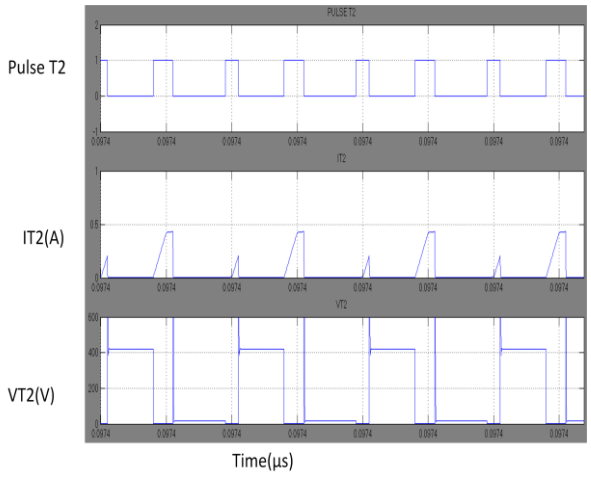

Fig.6 soft switching of the auxiliary switch

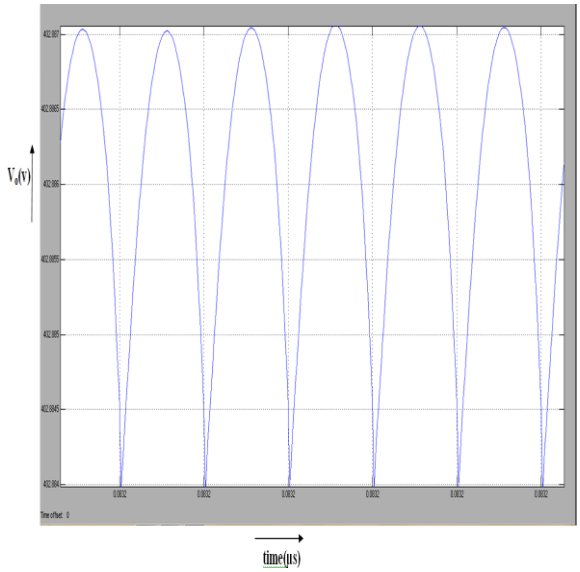

Fig.7 Ripple voltage waveform

Voltage across the main diode D_{F1}, D_{F2} is shown in the Fig. 8 and Fig. 9.

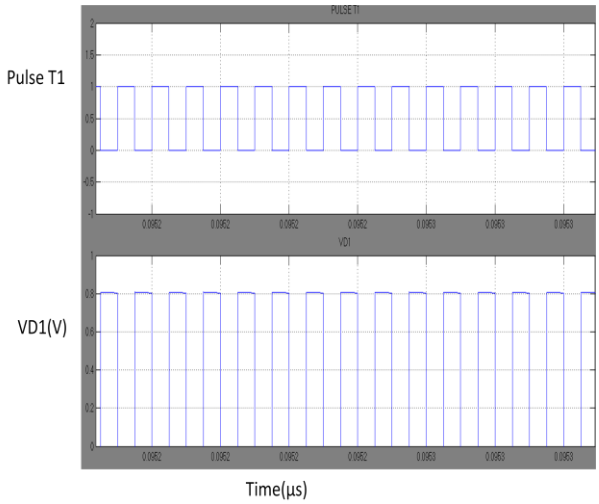

Fig. 8 pulse and voltage waveforms, T_1, V_{DF1}

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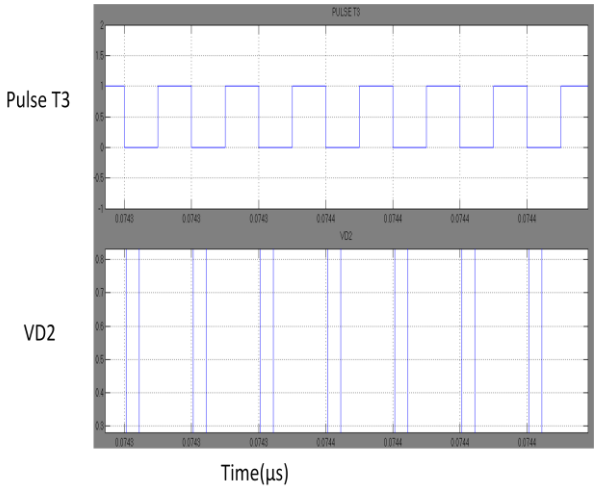

Fig. 9 pulse and voltage waveforms, T_2, V_{DF2}

V. CONCLUSION

Interleaved ZVT-ZCT PWM boost converter is proposed in this paper. Hence, the input current ripple is reduced and the voltage stresses of the switches are greatly reduced compared with the conventional boost topology. This leads to the significant reduction of the conduction losses. Also, the switching losses is reduced by using an active snubber cell which provides ZVT turn on and ZCT turn OFF together for the main switch of the converter. Also, the proposed snubber cell is implemented by using only one quasi-resonant circuit without an important increase in cost and complexity. In the proposed converter, all semiconductor devices are switched under soft switching. The main diode is not subjected to any additional voltage and current stresses. The operation principles and steady-state analysis of the proposed converter are presented. The proposed converter is analyzed, design considerations are discussed, and its various operating modes are presented. The proposed converter was more efficient than the conventional boost converter.

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