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SIMULATION OF HIGH STEP UP DC-DC CONVERTER FOR GRID TIE THREE PHASE INVERTER USINGRENEWABLE ENERGY

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ABSTRACT: This paper presents a high efficiency step-upDC-DC converter for low-DC renewable energy sources.The proposed DC-DC converter is controlled byasymmetrical pulse width modulation(APWM) techniqueand achieves Zero-current switching(ZCS) of all outputdiodes. Compared to the previous DC-DC converters, thevoltage stresses of the semiconductor devices can be reducedin the proposed converter. Simulation results areobtained from a 200 W output power. The proposed DC-DCconverter achieves a high efficiency of 97.5 % at the ratedload.Further project has been extended to three phase grid tie inverter using sinusoidal pulse width modulation technique.

Keywords*:*DC-DC converter, soft-switching, highvoltage gain, zero-current switching(ZCS),Three Phase Inverter.

I. INTRODUCTION

The power generation systems using low-DCrenewable energy sources such as photovoltaic moduleand fuel cell need a high step-up DC-DC converter tointerface the low-DC voltage to the high DC voltagedistribution network [1]. Lots of efforts have been madeto develop high step-up DC-DC converters with a highefficiency [2]-[6]. Among the investigated topologies, theactive-clamped step-up DC-DC converters in [4]-[6] aregaining its popularity, thanks to its high step-up ratio andsoft-switching operation. The active-clamped step-upDC-DC converters in [4]-[6] has a high step-up gain byusing the active-clamp circuit at the primary side and thevoltage doubler rectifier at the secondary side. Moreover,the series-resonance between the transformer leakageinductor and the capacitor in the voltage doubler rectifiermakes the output diodes to be turned off at zero currentcondition [5]. However, the power switches at theprimary side operate under hard-switching condition,which still causes high switching power losses and highheat dissipation problems. The half-bridge dc-dcconverter has been presented to reduce switching powerlosses at high-voltage side [1]. The output diodes areturned off at zero current by using the voltage doublerrectifier. However, an additional half-wave rectifier isneeded, which increases switching power losses.In order to overcome these problems, this paperproposes a high-simulation efficiency dc-dc converter for low-dcrenewable sources. An improved active-clamped dc-dcconverter is presented by using a dual active-clamping circuit. The voltage stress of power switches can bereduced at primary side. The performance of the proposedconverter is verified using a 200 W simulation prototype. The simulation results confirm that a highefficiency of 97.5 % is achieved at 50 V input voltage for200 W output power with an improved dynamic performance.

In this paper a new DC-DC converter topology is proposed to step up the fuel cell voltage and provide a stable dc-link for the DC-AC inverter. The proposed DC-DC power conversion unit consists of a two parallel connected buck-boost converters. This produces an independently controllable dual voltage output. Block diagram of proposed converter is shown in Fig.1. As it will be shown the use of the proposed topology along with a DC-AC inverter eliminates the need for a transformer to provide the required voltage gain. As a result, proposed topology has the following advantages:

- Operates from a single input voltage
- No transformer is required to achieve a voltage gain of 5 in per unit
- If a single phase is connected at its output the system can generate 230VAC output from a 50VDC input source without the use of a transformer.

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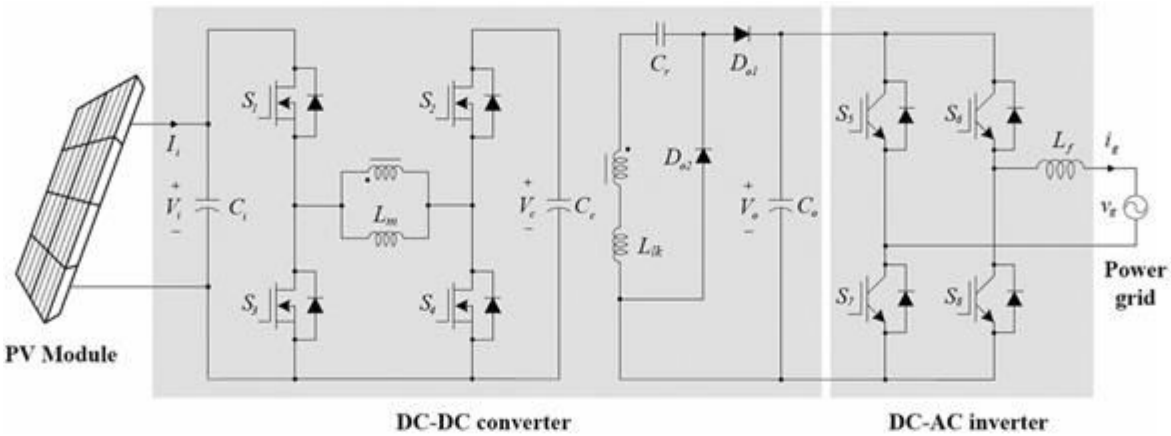

Fig.1: Proposed system configuration

II. INVERTER CONTROL SCHEME

The Fig. 1 shows the circuit diagram of the proposed stepupDC-DC converter. This converter combines an inputcapacitor *Ci*, a clamp capacitor *Cc*, main switches*S1* and*S4*, an auxiliary switches*S2* and *S3*, the resonant capacitor*Cr*, two output diode *Do1* and *Do2*, an output capacitor *Co*,and the secondary side leakage inductor *Llk*. Each switchhas its own parasitic capacitor *CS1* ~ *CS4* and body diode*DS1* ~ *DS4*. The switches operate at a constant switchingperiod *Ts*(= 1/*fs*) with the asymmetrical pulse-widthmodulation(APWM). The transformer *T* has themagnetizing inductor *Lm* and leakage inductor *Llk*with theturns ratio of 1 *: N* where *N* = *Ns*/*Np*. The proposedconverter operates in a continuous conduction mode sothat the magnetizing inductor current *iLm*flowscontinuously. The capacitors *Cc*, *Co* are large enough sothat their voltages are considered constant as *Vc*and *Vo*. *D*is the duty ratio based on *S1* (*S4*) turn-on time. Fig. 2(a)shows the operation waveforms of the primary sidecomponents. Fig. 2(b) shows the operation waveforms ofthe secondary side components. Fig. 3 shows theoperation modes of the proposed converter for *Ts*. The
proposed converter has six distinct operating modes for*Ts*as follows:

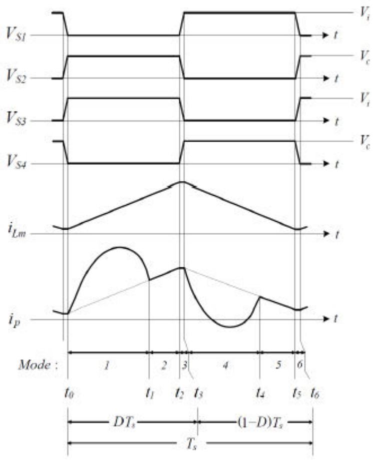

Fig.2(a): Voltage Waveforms of Switches

Mode 1 [t0, t1]: At *t* = *t0*, *S1* and *S4* are turned on. Since *VLm*= *Vi*, the magnetizing inductor current i_{Lm}increases linearly as

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$iLm(t) = iLm(t0) + Vi/Lm * (t - t0)$ (1)

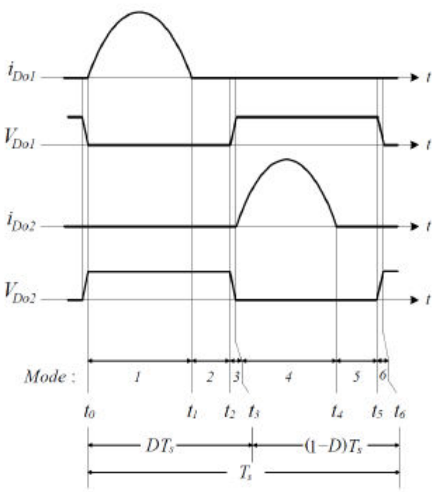

Fig. 2(b): Voltage and Current Waveforms across Diode

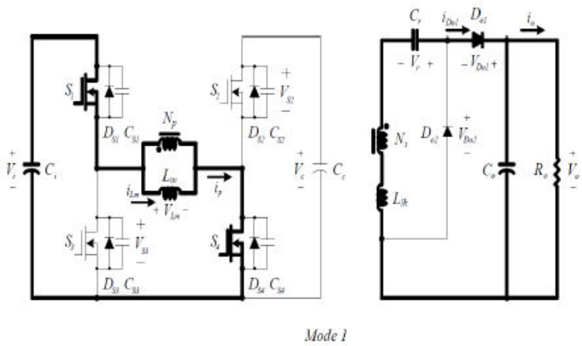

Fig.3(a): Mode -I

From $V = L\,di/dt \Rightarrow di = V/L * dt$ (2)

When $nVi$is applied to the secondary winding of Ns, the diodes $Do1$ is turned on. The series-resonant circuit consisting of $Llk$and Cr is formed, respectively. By the series resonance between $Llk$and Cr, the energy stored in the capacitor Cr is transferred to the output capacitors Co. The angular resonant frequency _r of this series-resonant circuit is

$w_r = 2\pi f_r = 1/\sqrt{L_{lk}C_r}$

where$fr$is the resonant frequency. By referring the output diode current $iDo1$ to the primary side, the primary current $ip$is expressed as

$ip(t) = iLm(t)$

$ip(t) = iLm(t) + niD01(t)$

$ip(t) = ip(t0) + \frac{Vi}{Lm} * (t - t0) + niD01(t)$ (3)

$iD01(t) = \frac{V0-nVi-Vr}{Zr} \sin wr(t - t0)$ (4)

Where Zr = $\sqrt{L_{lk}/C_r}$ (5)

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Mode 2 [t1, t2]: At *t* = *t1*, the half-resonant period for the output diode currents *iDo1* is finished. The output diode currents *iDo1* is zero before *Do1* is turned off. Zero current switching of *Do1* is achieved without any diode reverse recovery problem at the end of *Mode 2*.

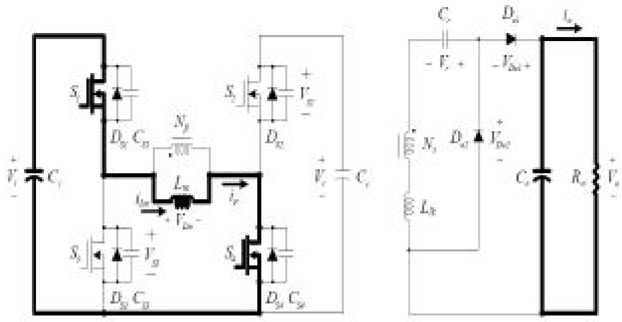

Fig.3(b): Mode -II

Mode 3 [t2, t3]: At *t* = *t2*, *S1* and *S4* are turned off. The primary current *ip*charges *CS1* and *CS4,* discharges *CS2* and *CS3*. The voltage *VS1* across *S1* increases from zero to the voltage *Vi*and The voltage *VS4* across *S4* increases from zero to *Vc.* Since the capacitor *CS* (= *CS1* = *CS4*) is very small, the time interval during this mode is considered negligible compared to *Ts*.

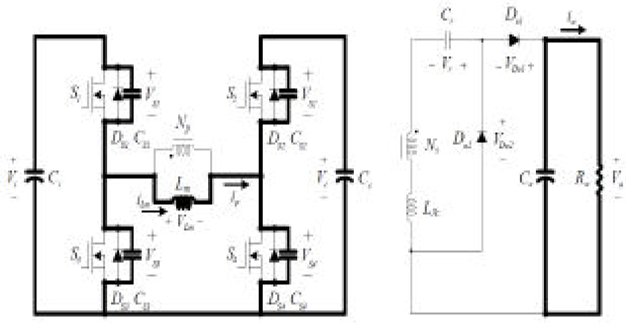

Fig.3(c): Mode -III

Mode 4 [t3, t4]: At *t* = *t3*, the auxiliary switches *S2* and *S3* are turned on with zero voltage. Thus, switching loss is reduced. Since *VLm*= –*Vc*, the magnetizing inductor current *iLm*decreases linearly as

$$iLm(t) = iLm(t3) - \frac{Vc}{Lm} * (t - t3) \qquad (6)$$

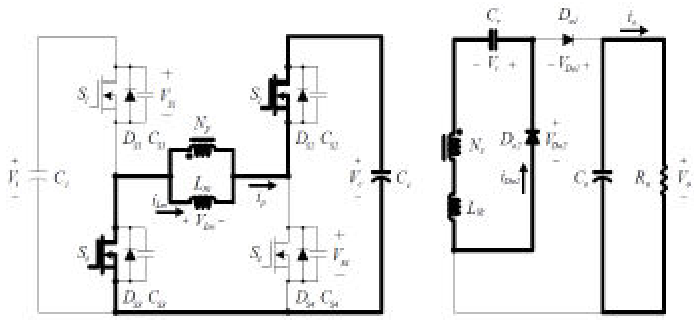

Fig.3(d): Mode -IV

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When $-nVc$is applied to the secondary winding of *Ns*, the output diode *Do2* is turned on. The series-resonant circuit consisting of *Llk*and *Cr* is formed, respectively. Through the output diode *Do2*, the energy is transferred to the resonant capacitor *Cr*. By referring the output diode current *iDo2* to the primary side, the primary current *ip*is expressed as

$$ip(t) = \ ip(t3) - \frac{Vc}{Lm} * (t - t3) - niD02(t) \qquad (7)$$

where the output diode current *iDo2* is given by

$$iD02(t) = \frac{nVc+Vr}{Zr} \sin wr(t - t0) \qquad (8)$$

Mode 5 [t4, t5]: At *t* = *t4*, the half-resonant period of the output diode currents *iDo2* is finished. The output diode current *iDo2* is zero before *Do2* is turned off. Zero-current switching of *Do2* is achieved without any diode reverse recovery problem at the end of *Mode 5*

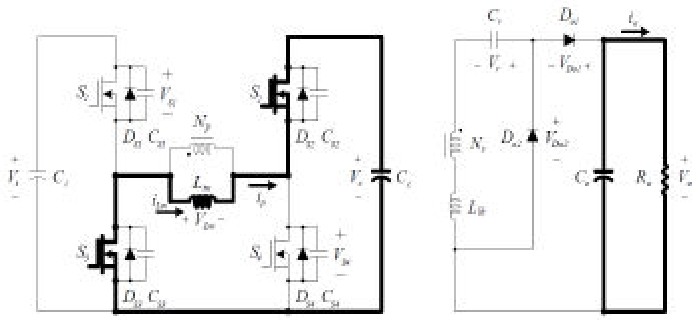

Fig.3(e): Mode -V

Mode 6 [t5, t6]: At *t* = *t5*, *S2* and *S3* are turned off. The primary current *ip*charges *CS2* and *CS3,* discharges *CS1* and *CS4*. The voltage *VS2* across *S1* increases from zero to the voltage *Vc*and The voltage *VS3* across *S3* increases from zero to *Vi*. Since the capacitor *CS* (= *CS2* = *CS3*) is very small, the time interval during this mode is considered negligible compared to *Ts*. The next switching cycle begins when *S1* is turned on again. By imposing the voltage-second valence role on the magnetizing inductor *Lm*, the capacitor voltages *Vc*, and *Vr*can be expressed as

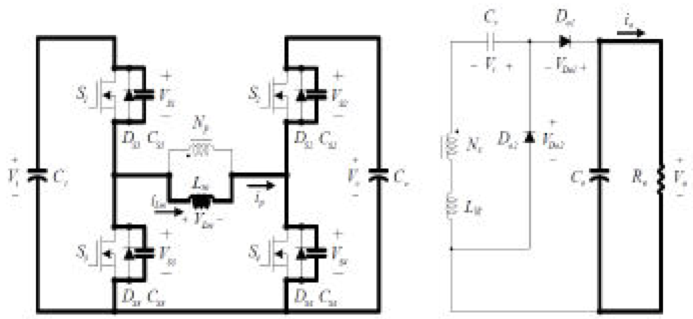

Fig.3(f): Mode -VI

$$Vc \ = \frac{D}{1-D} Vi \qquad (9)$$

$$Vr \ = \frac{n\text{^}2Lm - Lm}{nLm} \frac{D}{1-D} Vi \qquad (10)$$

where*D* is the duty cycle of the main switches *S1* and *S4*. For *Llk*<<*Lm*, (9) can be rewritten asfor voltage-second rule on the secondary winding, the following equations can be obtained.

$$Vr \ = \frac{D}{1-D} nVi \qquad (11)$$

(V*o*-*V r*)DTs = *nVc*–(1*D)Ts* *(12)*

From 9, 10, 11, 12 we have

$$Vo \ = \frac{n}{1-D} Vi \qquad (13)$$

The maximum voltage stress of *S1* and *S3* is confined to the input voltage *Vi*. The voltage stress of *S2* and *S4* is confined to the clamping capacitor voltage *Vc*. Fig. 4 shows the relation between the clamping capacitor voltage *Vc*and the duty ratio *D*. The dual active-clamping circuit is used in the proposed converter. The clamping capacitor voltage in case of the dual active-clamping circuit is always lower than the clamping capacitor voltage in case of the conventional active-clamping circuit. It means that the switch voltage stress of the proposed converter is always lower than the switch voltage stress of the previous converter [4] using the conventional active-clamping circuit. Especially, when the duty ratio is below 0.5, the clamping capacitor voltage can be lower than the input voltage *Vi*. It is critically beneficial in low-voltage PV applications where more than 50 % of the power losses are lost as switching power losses. The output diode currents *iDo1* and *iDo2* should be zero.

III. SIMULATIONRESULTS

Fig. 4 shows the Simulink model of the proposed converter and Fig. 5, 6 shows the primary current *ip*and output voltage of DC-DC converter, Fig. switch voltages*VS1* and *VS3* for 200 W output power. Fig. 5shows the simulation waveforms at 50 V input voltage.As shown in Figs. 5, *VS1* and *VS3* are clamped at the inputvoltage. Fig. 6 shows the primary current *ip*, clampingcapacitor voltage *Vc*, and switch voltages *VS2* and *VS4* for200 W output power. Fig. 6 shows the simulationwaveforms at 50 V input voltage. The clamping capacitorvoltage *Vc*is 48 V. *VS2* and *VS4* are clamped at 48 V.Fig. 8 shows the measured power efficiencies of theconverters at 50 V input voltage for different output loadconditions. The proposed converter achieves theefficiency of 97.5 % for 200 W output power. Theprevious active-clamped converter achieves the efficiencyof 97.2 % for 200 W output power. The efficiency of 0.3% is improved by the proposed converter at 50 V inputvoltage for 200 W output power. The previous halfbridgeconverter achieves the efficiency of 97.0 % for200 W output power. The proposed converter achievesthe highest efficiency for the rated output power.Switching power losses are reduced by decreasing thevoltage stress of power switches in the proposedconverter. The power efficiency is increased by reducingswitching power losses.

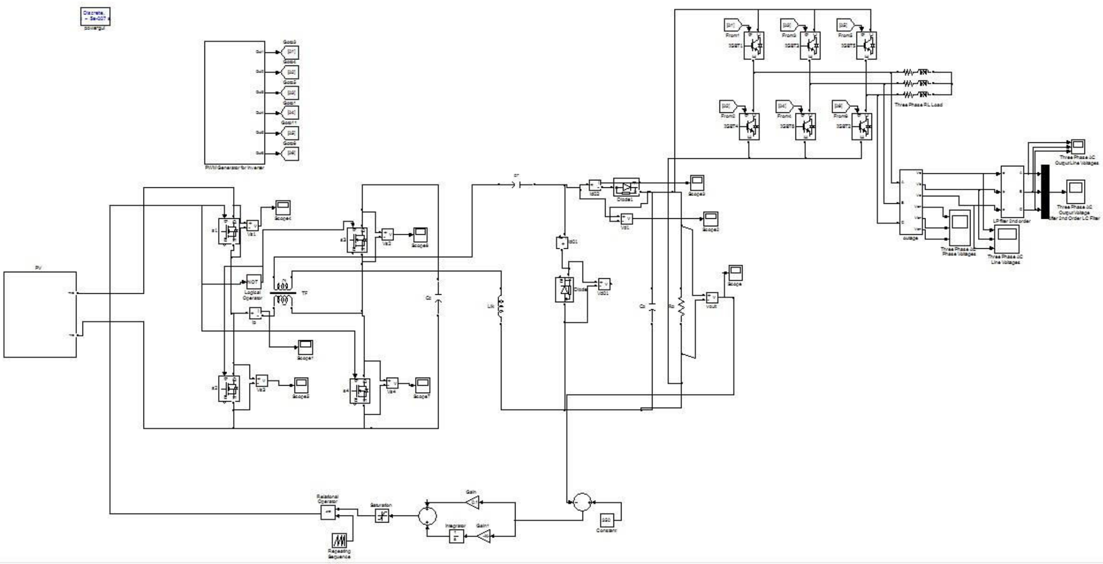

Fig.4: Simulink model of proposed converter

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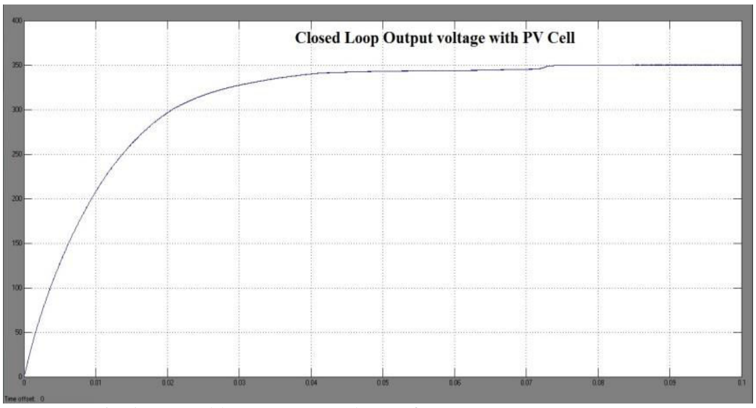

Fig.5: Control loop Output Voltage of step up DC – DC Converter

Fig. 7 shows the simulation waveforms for 200 W output power. The diode currentflows in a resonant manner by the series resonance between the leakage inductor and the resonant capacitor. The diode current is zero before the output diode isturned off. Zero-current switching of each output diode isachieved at its turn-off instance.

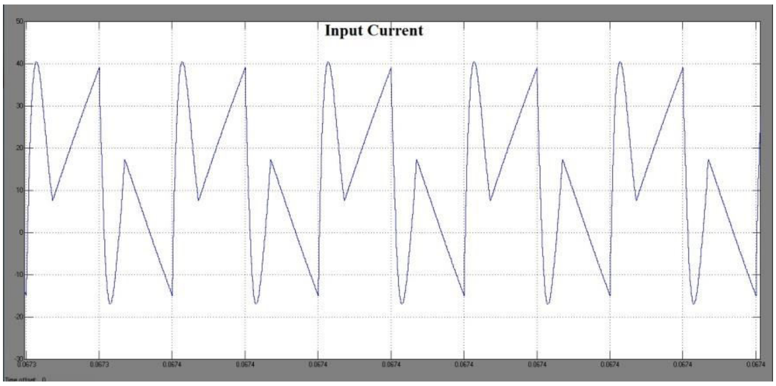

Fig. 6:Input current wave form of the DC-DC Converter

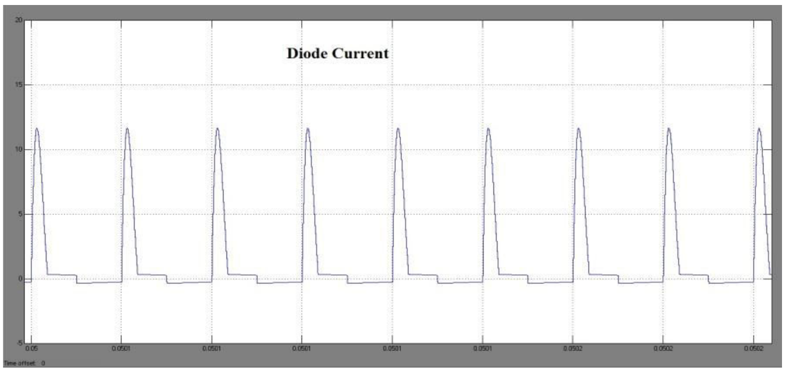

Fig. 7:Diode Current ID01

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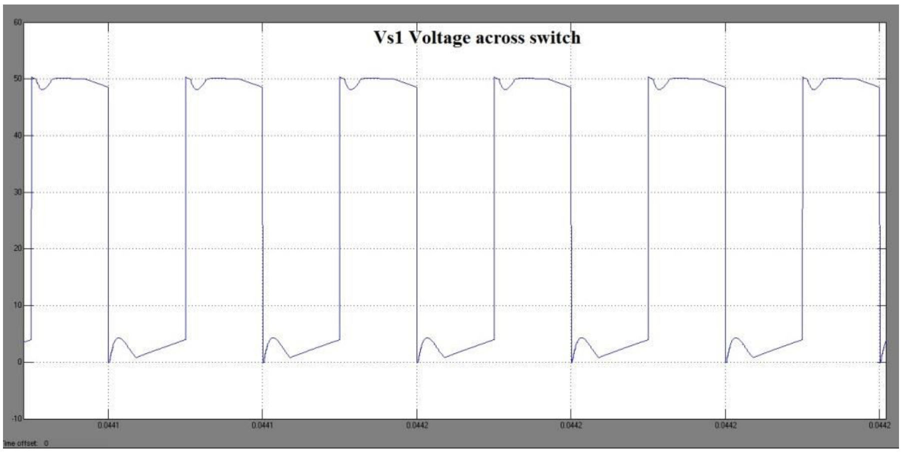

Fig. 8:Voltage Across Switch VS1

Fig. 8 shows the output diode voltages *VDo1* and *VDo2*and output diode currents *iDo1* and *iDo2* for different outputload conditions. The switching powerloss caused by the diode reverse recovery current can beremoved by zero-current turn-off of the output diode.

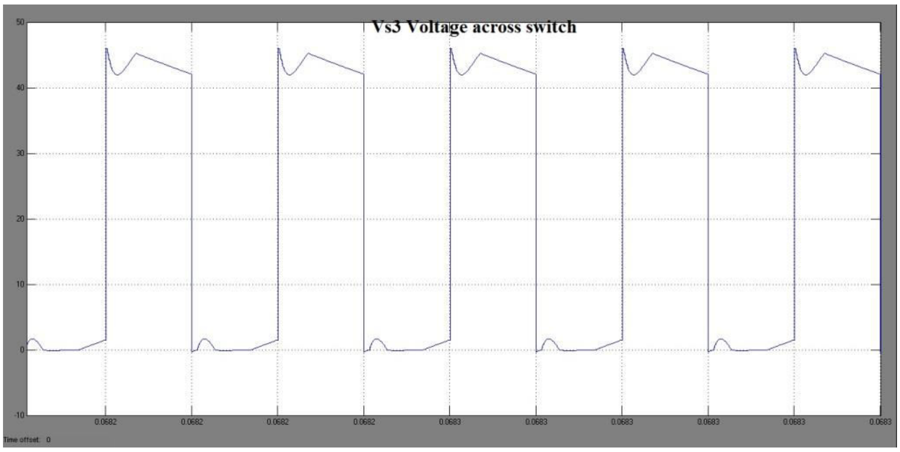

Fig. 9: Voltage Across Switch VS1

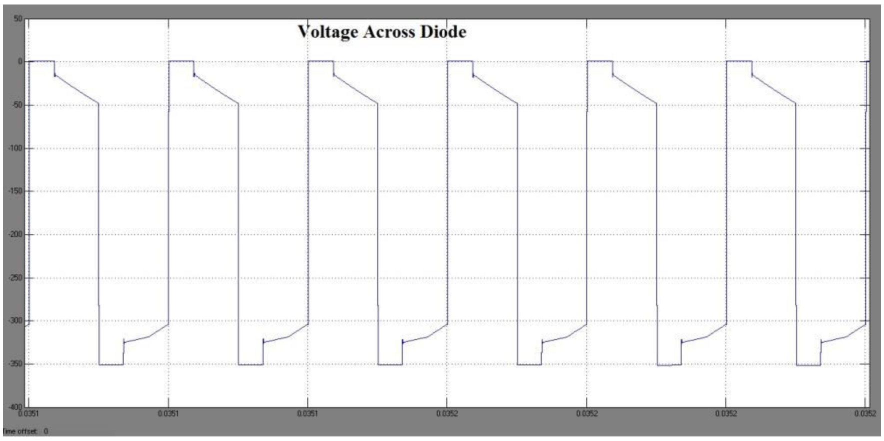

Fig. 10:Wave form of voltage across diode

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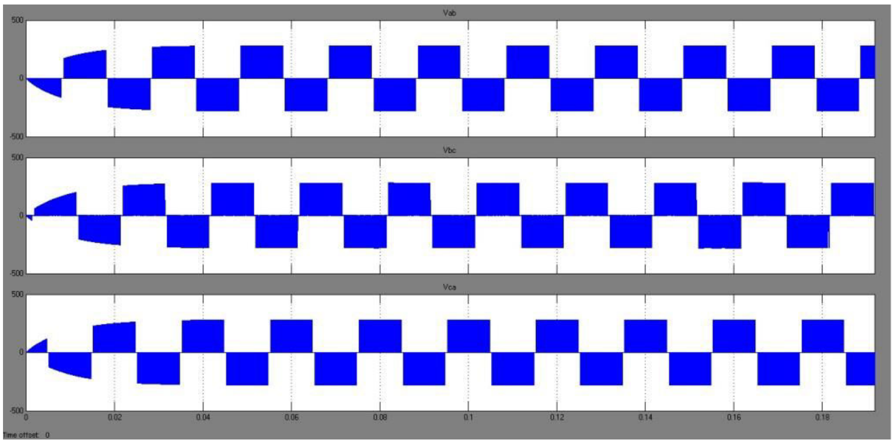

Fig. 11: Inverter output voltages before using filter configuration

Fig. 11 shows the output voltage of inverter and output voltage without filterfor different outputload conditions. The switching powerloss caused by the switching of three phase inverter causes the output voltage to be stepped waveform.

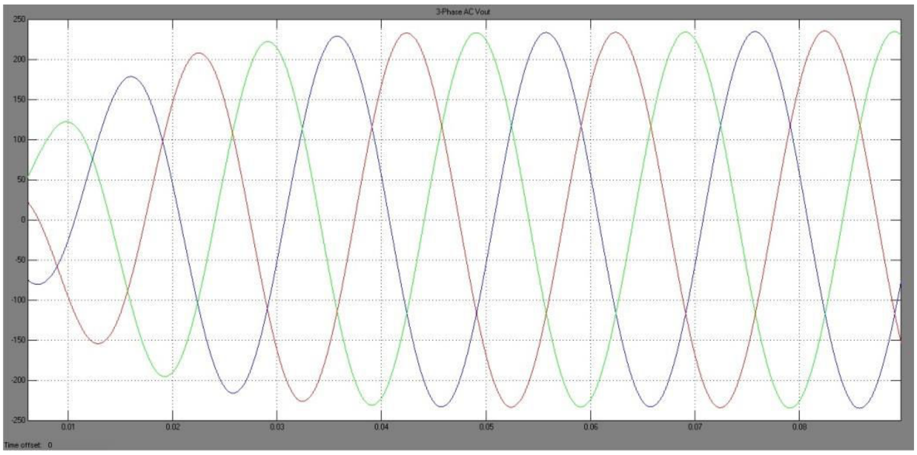

Fig. 12:Inverter output voltages after using filter configuration

Fig. 12 shows the output voltage of inverter and output voltage with filterfor different outputload conditions. The switching powerloss caused by the switching of three phase inverter causes the output voltage to be stepped waveform without filter and filtering causes the output voltage to be pure sinusoidal which is directly fed to the grid.

IV. CONCLUSION

This paper presents a high efficiency step-up DC-DCconverter for low-DC renewable energy sources. Theoperation of the proposed converter has been described.The simulation results has been presented at inputvoltage *Vi*= 50 V. The proposed converter reduces theswitching power losses, increasing power efficiency. Byusing series resonant circuit, the proposed converterachieves ZCS turn-off to remove the reverse-recoveryproblem on output diodes. Simulation results haveshown that the proposed converter achieves a high efficiency of 97.5 %. By feeding DC output voltage of converter to three phase grid tie inverter gives pure sinusoidal voltage with 50Hz frequency and suitable output AC voltage .

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BIOGRAPHY

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