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Study of MPLS over ATM Network

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ABSTRACT: MPLS is high lightened as the most promising technology for the ATM backbone network. This MPLS improves in reducing the traffic in the network and increases the bandwidth. ATM switch network for the fast Internet services which makes use of virtual network for switching between routers by adding a layer 3 routing module to the existing ATM network and can provide scalable Internet services to users with various service levels. This paper presents an implementation of MPLS for an ATM network on FPGA which replaces the virtual circuits by use of labels in the network.

Keywords: MPLS, Asynchronous Transfer Mode, Ingress packet processing module, Egress packet processing module.

I.INTRODUCTION

The exponential growth of the Internet over the past several years has placed a tremendous strain on the service provider networks. As we all know there has been an increase in the number of users with that there has been a multi-fold increase in newer applications, backbone traffic, connection speeds. At the start of communication ordinary data applications required only store and forward capability in a best effort manner. Now days there are many newer applications like voice, multimedia and real-time ecommerce applications are pushing toward higher bandwidth and services, irrespective of the dynamic changes or interruptions in the network.

To make the service level guarantees to the service providers not only have to provide large data pipes (Which are also costlier), but also look for architectures which can provide & guarantee QoS (quality-of-service) and optimal performance with minimal increase in the cost of network resources.

IP-based networks typically lack the QoS features available in circuit-based networks, such as ATM and Frame Relay. MPLS brings the sophistication of a connection-oriented protocol to the connectionless IP world. MPLS brings performance enhancements and service creation capabilities to the network. MPLS technology enables Internet Service Providers to offer additional services for their customers, scale their current offering, and exercise more control over their growing networks by using its traffic engineering capabilities.

Figure 1 shows that the MPLS is inserted between layer 2 and layer 3.

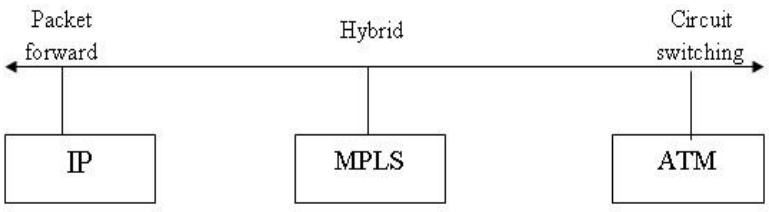

Figure 1 MPLS B/N IP and ATM

II.RELATED WORK

MPLS is comprised of different protocols, each performing a different task in the MPLS work flow. Each protocol have been researched differently with respect to hardware implementation. The work in [2] describes hardware implementation of IS-IS protocol. In [3] research on hardware implementation of OSPF protocol is discussed. Research

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in [4] and [5] discuss the hardware implementation of subset of RSVP-TE and CR-LDP protocols respectively. The work in [7] describes the hardware implementation of reconfigurable MPLS router.
The work in [6] has introduced a hardware processor for the implementation of MPLS using RSVP-TE as its signalling protocol. In [8], an embedded architecture for the MPLS protocol was proposed. The design uses both hardware and software to implement different aspects of MPLS. The architecture proposed implementing routing functionality in software, label switching functionality in hardware.

III.MPLS AND ATM

MPLS

IP-based networks typically lack the quality-of-service features available in circuit-based networks, such as ATM and Frame Relay. MPLS replaces the virtual circuits (VC) which reduces the hardware components for connection between routers in the ATM network. MPLS provides an increase in the performance enhancements and service creation capabilities to the network.
MPLS stands for Multiprotocol Label Switching here are some of the terms which are used extensively in MPLS
1. Forwarding Equivalence Class (FEC): a group of IP packets which are forwarded in the same manner (e.g., over the same path, with the same forwarding treatment).

2. MPLS header: The 32-bit MPLS header contains the following fields:
   i. The label field (20-bits) carries the actual value of the MPLS label.
   ii. The Experimental bits (3-bits) can affect the queuing and discard algorithms applied to the packet as it is transmitted through the network. Since this field has 3 bits, therefore 8 distinct service classes can be maintained.
   iii. The Stack field (S) (1-bit) supports a hierarchical label stack. This MPLS supports the processing of a labelled packet is always based on the top label. An unlabelled packet can be thought of as a packet whose label stack is empty (i.e., whose label stack has depth 0). If a packet's label stack is of depth n, we refer to the label at the bottom of the stack as the level 1 label, to the label above it then as the level 2 label if such exit, and to the label at the top of the stack as the level n label. The label stack is used for routing packets through LSP Tunnels.
   iv. The TTL (time-to-live) field (8-bits) provides conventional IP TTL functionality.

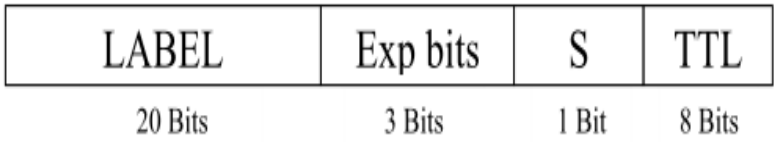

Figure 2 MPLS header format

ATM- Asynchronous Transfer Mode

A high performance cell oriented switching and multiplexing technology that utilizes fixed length packets to carry different type of traffic. It contains voice, data and video signals. It was designed for a network that must handle both traditional high-throughput data traffic (e.g., file transfers), and low-latency content, real-time such as voice and video.

ATM is a core protocol mainly used over the SONET/SDH backbone of the public switched telephone network (PSTN) and Integrated Services Digital Network (ISDN).

Structure of an ATM cell
An ATM cell is of 53 bytes which consist of 5-byte header and a 48-byte payload.
GFC = Generic Flow Control (4 bits)
(Default: 4-zero Bits)
VPI = Virtual Path Identifier (8 bits UNI) or
(12 bits NNI)
VCI = Virtual Channel identifier (16 bits)
PT = Payload Type (3 bits)
CLP = Cell Loss Priority (1-bit)
HEC = Header Error Control

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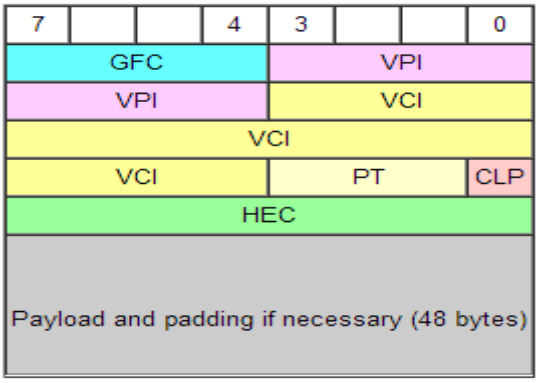

Figure 3 UNI ATM cell

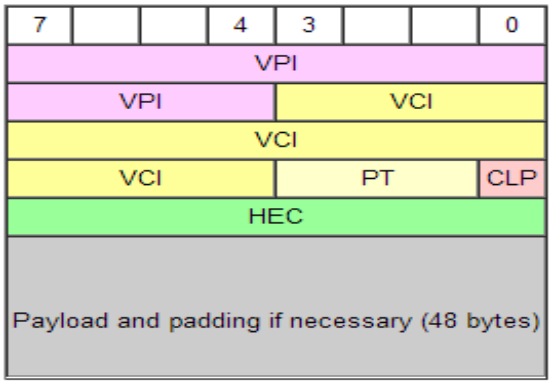

Figure 4 NNI ATM cell

IV.ARCHITECTURE FOR MPLS

The MPLS packet processing includes label lookups, packet forwarding, label manipulation and routing protocol functionality. Below figure illustrates a high level description of MPLS architecture

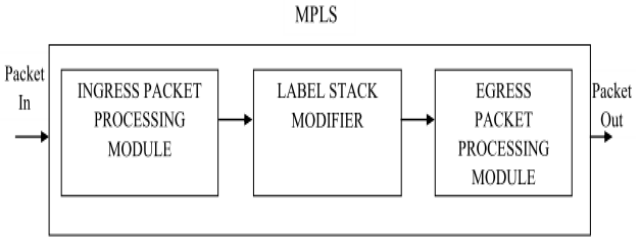

Figure 5 MPLS Architecture

The architecture consists of two packet processing modules, and a separate module to modify the label stack. Ingress packet processing module will process the packet and separate the label with the packet, in the label stack modifier will replace the label with new label. The packet with the new label will transfer to the next router, the egress packet processing module is the last router before the destination will process the packet and then it will remove the label from the packet and transfer packet with no label to the destination. Label and an Egress LER has not outgoing label. Those values are presumed to be zero.

A. Ingress Packet Processing Module

The input to Ingress packet processing module is the incoming packet with a valid destination address. When the packet arrives the packet processing unit separates the address and the data part. The data is stored in the data buffers while the control information is passed on to next unit for verifying its correctness. If the packet received is valid then it is passed on to label stack modifier where the labels are modified based on the control information available. If the packet received is invalid then the packet is drop.

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The following Figure shows the flowchart of the ingress packet processing module.

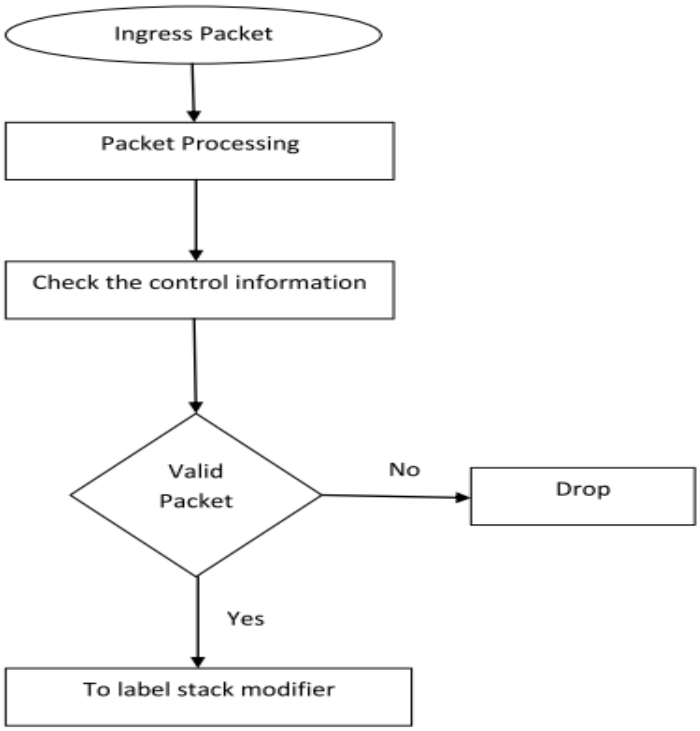

Figure 6 Ingress packet processing module flowchart

B. Label Stack Modifier

The control unit of the label stack modifier is composed of four state machines. Those state machines are the label stack interface, information base interface, information base search module and main module illustrated in below Figure.

The main module is used to ensure that the remaining state machines are not working concurrently and generating inconsistent results. When the main module is not active, it has enabled the label stack interface or the information base interface and waits for the module in question to finish its activity before allowing subsequent operations to happen.

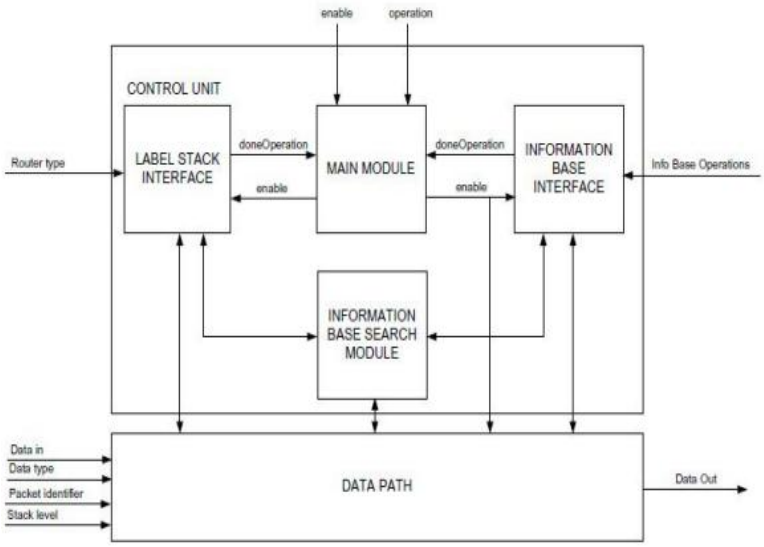

Figure 7 Label stack modifier architecture

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The label stack interface is used to insert label entries directly into the stack and to update the stack given the existing state of the information base. The packet is discarded (i.e. the label stack is reset) if the relevant entries are not found in the information base or if the TTL has expired. Updating the label stack involves searching the information base for the desired new label (if necessary) and operation. If information is found the top entry in the stack is removed and the TTL is updated before information is verified. If there are any inconsistencies in the information or if the TTL is expired, the packet is immediately discarded.

The information base interface remains idle until it is enabled by the main module and proceeds to either search or save data to the information base. To search the information base, the search module is enabled. Once the operation is complete a transition back to the idle state occurs where the information base interface indicates that the operation has completed. The search module is enabled by either the label stack interface or the information base interface. Once it has been enabled, the search module iterates through the label pair entries of a specified level. External data enters the data path and is interpreted as a label stack entry, a label pair (old label/new label) for the information base or a search index when the user wants to read the contents of the information base directly. Label stack entries can be stored from external data or from a register that holds the label entry currently being modified.

C. Egress Packet Processing Module

The Egress Packet Processing Module gets the input from label stack modifier for further processing of the packets. Figure 8 shows the flowchart of Egress Packet Processing Module. The Egress Packet Processing Module constructs the header as per the required format and replaces the fields such as TTL and CRC based on the control information. The packet generator block basically construct the packet by padding the data and control information together. Then the packet is sent to data buffer for forwarding through the output ports.

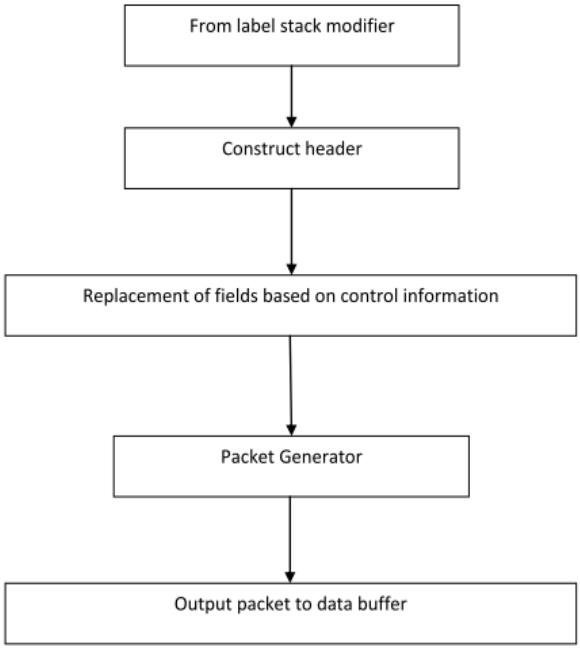

Figure 8 Egress packet processing module flowchart

V.CONCLUSION

ATM network is a connection oriented which gives better quality-of-service features available in circuit-based networks. MPLS over ATM network replaces the VC by inserting a label in each packet and forwards the packet with label throughout network which performs as connection-oriented protocol from this it maintains the QOS. Based on simple improvements in basic IP routing, MPLS increases performance enhancements and service creation capabilities to the network. So ATM with MPLS usage into the enterprise can meet emerging requirements for scalable transport for end user services, including data, voice and video.

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BIOGRAPHY

Satish M B currently pursuing his Post graduate degree in VLSI and Embedded systems from Sri Siddhartha Institute of Technology, he received his Bachelor degree in Telecommunication Engineering from Visvesvaraya Technological University, Belgaum, Karnataka, India. His research interests are in the areas of VLSI Design, ASIC Design, Micro-controller 8051.

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