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VLSI Design of Low Power Fault Detection in SRAM using BIST

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Abstract: Static Random Access Memory (SRAM) has become a key factor in new modern VLSI systems. Memories become more vulnerable to faults when the complexity of these memories increase as the technology shrinks. This detection of faults in SRAM has been a time consuming process. Hence transient current testing methods are used. This paper implements a transient current testing method to detect faults in Complementary MOSFET (CMOS) SRAM cells. By monitoring a transient current pulse during a write operation or a read operation, faults can be detected. In order to detect the fault, a Built in self-test (BIST) circuit is developed. Simulations are carried out on a 13T SRAM circuit, to detect the difference in waveform. To minimize the testing power in 13T SRAM were designed using transmission gates. It can be simulated using 0.25 µm CMOS process technology and also compared their simulation results with 6T SRAM cell. These qualities of the proposed design make it for high performance memory chips in the semiconductor industries.

Keywords: SRAM; CMOS integrated circuit; Transmission gates; BIST

I. INTRODUCTION

Embedded memories are popular in the realization of today's complex systems known as system on chips (SOCs). The forecast for 2013 from International Technology Roadmap for Semiconductors (ITRS) states that 90% of the area of SOCs will be made up of memories most specifically static random access memories (SRAMs) Large arrays of fast SRAM help in expanding the system performance. However, this increases the chip cost. Thus for area cost optimization the size of SRAM cells are minimized. Thus, small SRAM cells are closely placed making SRAM arrays the densest circuitry on a chip. Such areas on the chip can be vulnerable to manufacturing defects and process variations. This implies that test cost of memories will make a large impact on the test cost of the SOCs. The faults in memories result in reduction of yield. In critical systems these may cause system‘s failure. Thus adequate test methods must be employed in order to minimize the cost while maintaining efficiency thereby increasing the quality of the product. In a SRAM testing, various fault models such as stuck-at, transition, coupling faults are used. In order to detect these faults, March tests has been widely used. But these detection processes are time consuming. Testing using quiescent current (IDDQ) is also used . However, some defects in SRAM cells may not be detected using IDDQ. This project proposes a transient current testing method to detect open defects in CMOS SRAM cells. By monitoring a transient current pulse during a write operation or a read operation, faults can be detected [1-4].

II. EXISTING 6T SRAM CELL

The Numerous types of SRAM designs are used like 4T SRAM Cell, 6T, 7T, 8T, 9T etc. for various applications, but the commonly embedded design of SRAM in a microprocessor or SoC's is based on 6T SRAM cell. In 6T SRAM cell two inverters are back coupled with access transistors to hold the binary bits. The power consumption in 6T SRAM Cell is low, compared with other configurations, due to low leakage currents. Also the regenerative property of back-couple inverter cells provide strong logic levels and high data stability is achieved (Figure 1) [5,6].

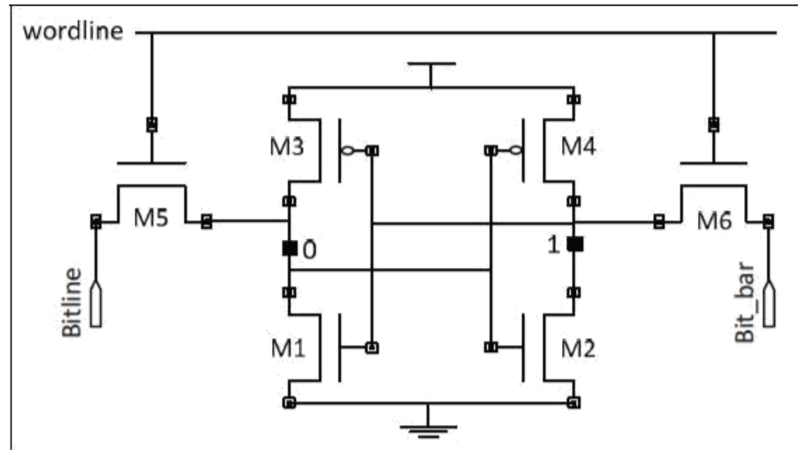

Figure 1: Existing 6T SRAM cell.

To properly read and write operations the width to length ratio of each MOS transistor is carefully calculated keeping various factors in consideration. For proper write operation or write stability the voltage across the access transistor (M6),connected to Bit bar line should be less than threshold voltage which turn 'OFF' the access transistor (M6) so that bit line write the binary bit '1' in memory cell keeping Bit line access transistor (M5) in 'ON' state.

A.Hold Mode

In hold mode, WL and BL lines are disabled. The transistors are in isolated condition it holds the data in Q node.

B.Read Mode

In read operation BLB are enabled which provides discharging path for through transistors. Depending on the data stored at QB. The disabled WL makes data storage nodes (Q and QB) decoupled from BL during the read access.

C.Write Mode

For writing data into the cell, WL is activated to transfer the data to storage node from BL, which is set/reset according to the data to be written. BLB is disabled.

III. PROPOSED 13T SRAM DESIGN

The proposed work is enchanced design and simulation of 13T configuration to study its behaviour in nano scale technology node using simulation software Tanner EDA Tool. The schematic of the proposed design will be based on modifying the existing SRAM Cell configurations. The various parameters for the design of power and performance metric based on power can be considered for developing the proposed SRAM Cell (Figure 2).

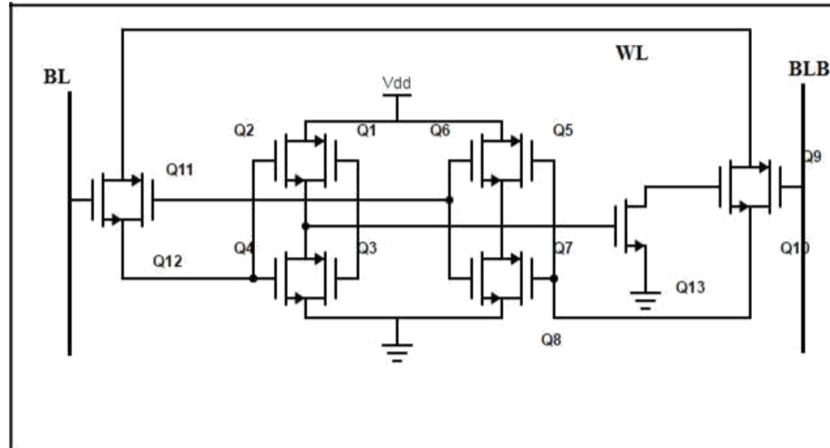

Figure 2: Proposed 13T SRAM design.

The gate leakage current based power dissipation, effect of performance metric will be analyzed by making use of simulated. The ST based 13T Static-RAM cell consists of a cell core (cross-coupled inverter), a read path consists the two transistors, read and a Write-Access (WA) transistor. The architectural change in the proposed schematic is the use of transmission gates in the access path. The transmission gate passes over the entire voltage range, i.e., strong ‘0’ and strong ‘1’ which improves the optimization of the designed SRAM Cell will also be carried out for low power, low delay design. The write-access transistor is controlled by row-based Word Line (WL), and the read-access transistor is controlled by BLB. The feedback transistors of ST nearby Q5 and Q6. Here to minimizes the power dissipation. BIST methods are used to reduce the power consumption of the circuit [7-9].

A. Transmission Gate

The proposed 13T SRAM was designed with transmission gates for reducing power. A transmission gate is similar to a relay that can conduct in both directions or block by a control signal with almost any voltage potential. It is CMOS based switch in which PMOS passes a strong 1 but poor 0 and NMOS passes strong 0 but poor 1. Both PMOS and NMOS work simultaneously. The main purpose is used to reduce the power in circuit.

B. Precharge Circuit

The pre-charge circuit is used just before the initiation of the read operation. The pre-charge circuit charges the bit line and bit bar line with the same potential and it forces so that during read operation the potential of either bit-line or bit-bar line discharge through NMOS transistor of the SRAM cell inverter which holds the binary ‘1’ value at its input (Figure 3).

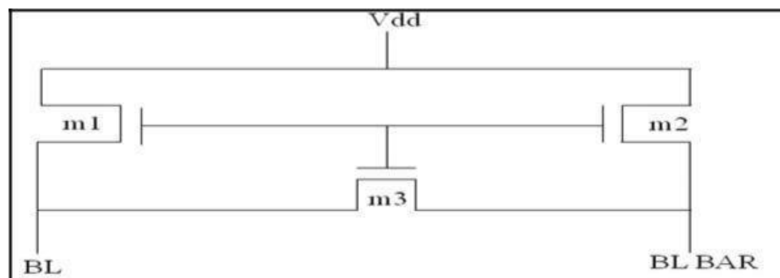

Figure 3: Precharge circuit.

C. Sense Amplifier

Sense amplifier is a regenerative structure like a latch which speeds up the generation of the output. It is basically a simple regenerative differential amplifier. It compares the difference between the voltage levels of bit and bit bar lines (Figure 4).

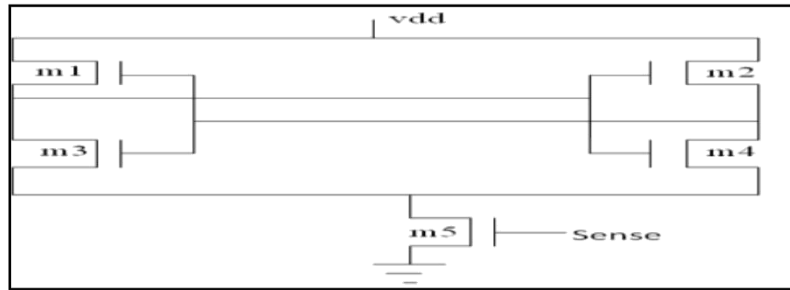

Figure 4: Sense amplifier.

In this sense amplifier m5 transistors are sense any changes its output even with small difference between the bit lines. The sense amplifiers are coupled to the bit lines through two switches which are enabled only during a short period of read time. Then the data is latched.

IV. BUILT IN SELF TEST ARCHITECTURE (BIST)

Built in Self-Test is additional low cost, effective integrated circuit incorporated with SRAM memory to test the occurrence of any possible fault during read write operation of memory (Figure 5).

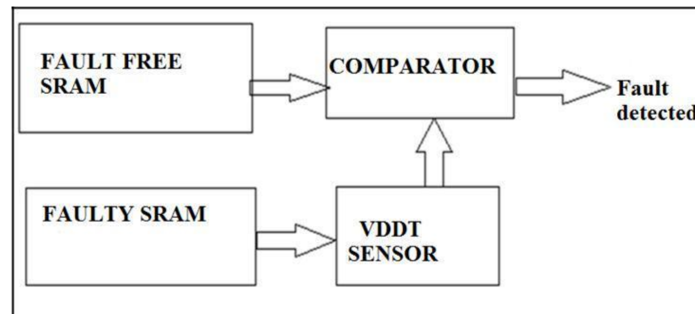

Figure 5: Block diagram of built in self-test architecture (BIST).

Thus the use of expensive and time consuming external hardware block called Automated Test Equipment is eliminated. It has several features compared to external ATE; it has fast and inexpensive testing of SRAM with covering all the possible manufacturing or, electrical fault on expense cost of the area and the power consumption.

A. Fault Introduced

Fault occurs in SRAM due to logical or electrical design error, manufacturing defects, aging of components, or destruction of components or process variations. Manufacturing defects are defects that were not intended. A manufacturing defect can occur despite of careful design. The size of memory causes physical examination of SRAM impossible. Thus testing mechanism is based on the comparison of logical behaviour of faulty memory against good memory. To compare logical behaviour of faulty memories against good ones, modelling the physical failure mechanisms as logic fault models is required. The failure in SRAM occurs due to open and bridging faults. Open fault occurs where two nodes which are supposed to be connected is left open and they can be modelled as a high resistance connected between those particular nodes. Bridging fault [10,11]. It is modelled as a low valued resistance connected across two nodes to show the shorting of the nodes which are supposed to be open. Thus any resistances shown above can be introduced into a SRAM to make it faulty. The values of resistance used are given in Table 1. It also states the nature of that particular fault. The established logic fault models in SRAM are listed below.

Resistance	Resistance Value (Ω)	Nature of fault
R1	1 MΩ	Open defect 1
R2	1 MΩ	Open defect 2
R3	1 MΩ	Open defect 3
R4	1 MΩ	Open defect 4
R5	1 MΩ	Open defect 5
R6	1 MΩ	Open defect 6
R7	10 Ω	Bridging defect 1
R8	10 Ω	Bridging defect 2
R9	10 Ω	Bridging defect 3
R10	10 Ω	Bridging defect 4
R11	10 Ω	Bridging defect 5

Table 1: The values of resistance used.

B. VDDT Sensor

IDDT current is a very fast action, it is extremely difficult to sense and process it. Mostly in low power technologies, processing the dynamic supply current is almost insoluble. Thus by transforming the current to voltage, and then handling the resulted voltage waveform is a possible solution. A VDDT sensor is shown in Figure 3. The output voltage keeps the shape of the dynamic current, but M2 and M5 act as two emitter followers, which have the same DC conditions resulting from the fact, that since M1 is larger compared to transistors in the cell and that the gate of M1 is grounded, the voltage drop on it is nearly zero. Thus, the gate of M2 can be considered as connected to VDD, just like the gate of M5. Currents through M5 and M2 are also identical and hence, transistors have the same DC conditions. This way stable DC conditions are ensured on the differential pair (M6- M7) as well. The role of capacitor C is to stretch the voltage waveform in node Vsense. The main requirement for this circuitry is good device matching. Output of the differential amplifier is connected to an opamp of high gain hence then transient voltage in µV can be transformed to mVolts and Volts A fault-free SRAM cell draws no significant supply current in a steady state, which means quasi zero static current. Substantial supply current is only driven when the cell is changing its state causes a current flow for the time of the switching, which is called the dynamic or transient current This current is sensed by pmos M1. This sensed voltage is given in V (SENSE). Small spikes of µV range appears in the waveform V (SENSE). This transient voltage is sent to the differential pair. With good device matching of differential an approximately equal output is made at the output nodes. These two outputs are given to a high gain opamp. The voltage is at V range, and could be processed easily. are stretched in time. This stretch in time is useful for further processing.

C. Testing of SRAM in BIST Circuitry

A fault free SRAM cell along with the Vddt circuitry, a faulty SRAM cell, an opamp and a comparator is shown in Figure 4. The faults introduced here can be open faults or bridging faults. The outputs from the opamps of faulty and fault free circuit is compared using the comparator. And if there is any fault in SRAM the outputs of opamps will vary due to the change in transient current change. And hence a pulse is obtained at the output of comparator. Instead of a SRAM cell an array of cells can also tested with this same circuitry [12,13].

IV. SIMULATIONS AND RESULTS

The simulation results for Power Minimized 13T SRAM using power gating clock gating techniques presented in this section.

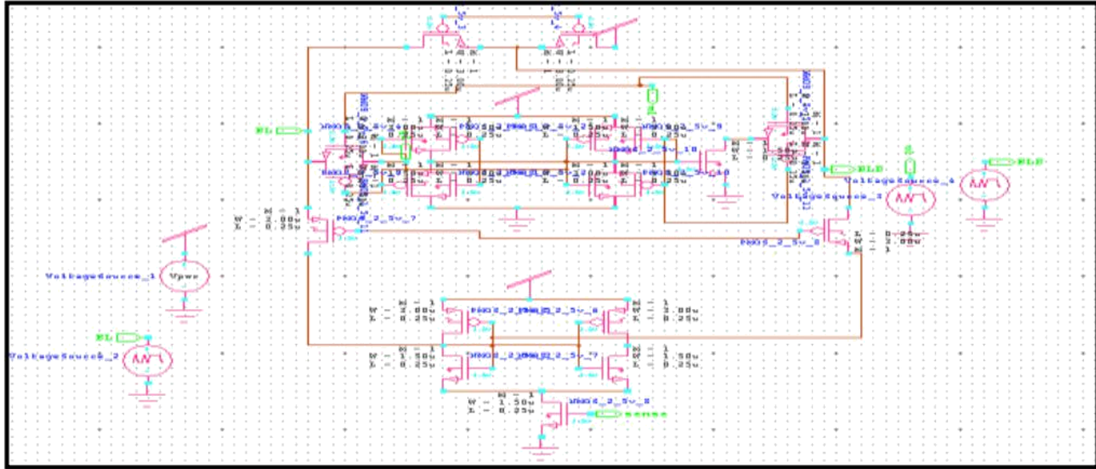

Figure 6: Schematic diagram for 13T SRAM (FAULT FREE) using transmission gates.

Figure 6 shows that Simulation results for 13T SRAM using Power gating. Here the sleeping transistors are added at header of the circuit for reduction of power in 13T SRAM design.

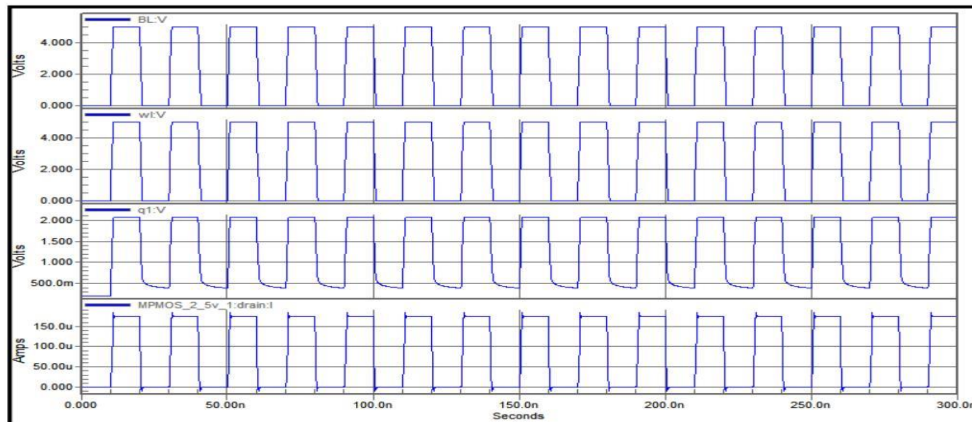

Figure 7: Simulation result of 13T SRAM using power gating for write operation.

Figure 7 shows that simulation result of 13T SRAM using power gating for write operation when BL and WL are enable then q node are charging.

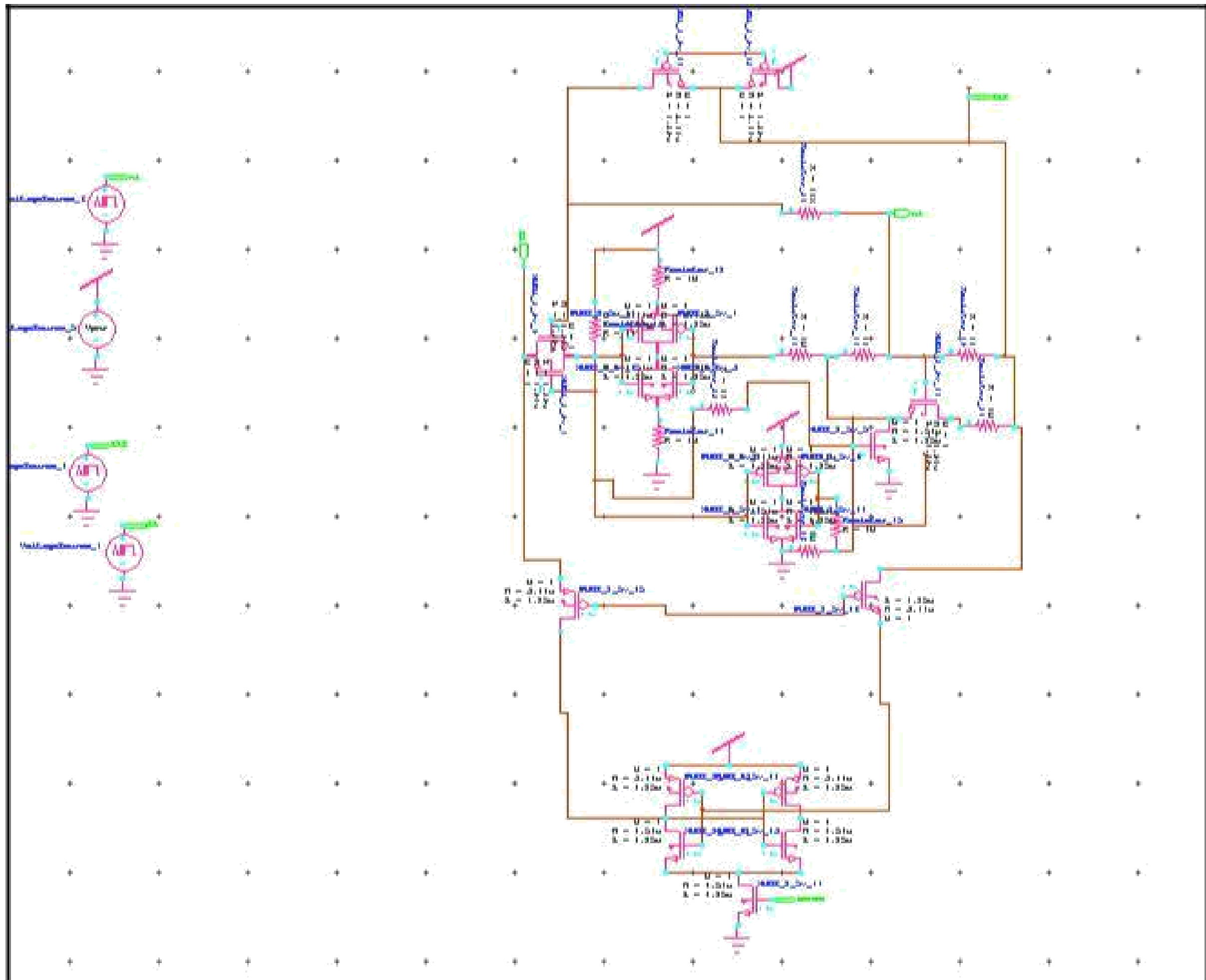

Figure 8: Schematic diagram of 13T SRAM(FAULTY) using transmission gates.

Figure 8 shows that schematic diagram using clock gating which represent the NOR gate are used in 13T SRAM for reducing switching activity [14,15].

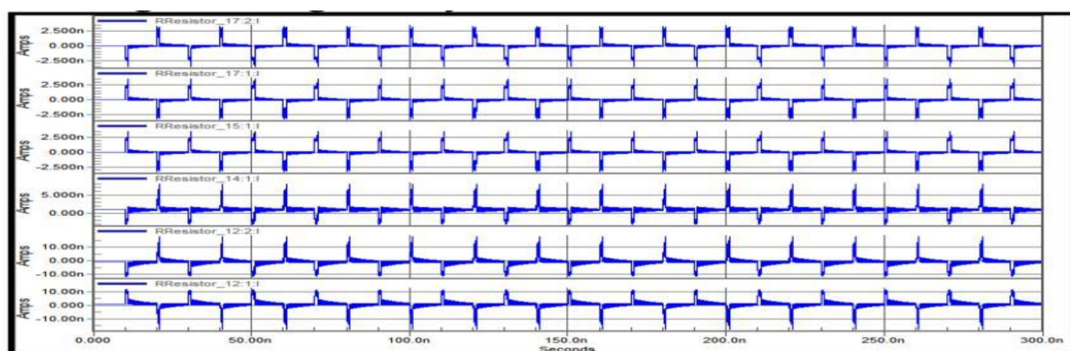

Figure 9: Simulation result 13T SRAM (FAULTY) using transmission gates.

Figure 9 shows that simulation result 13T SRAM (FAULTY) using transmission gates.

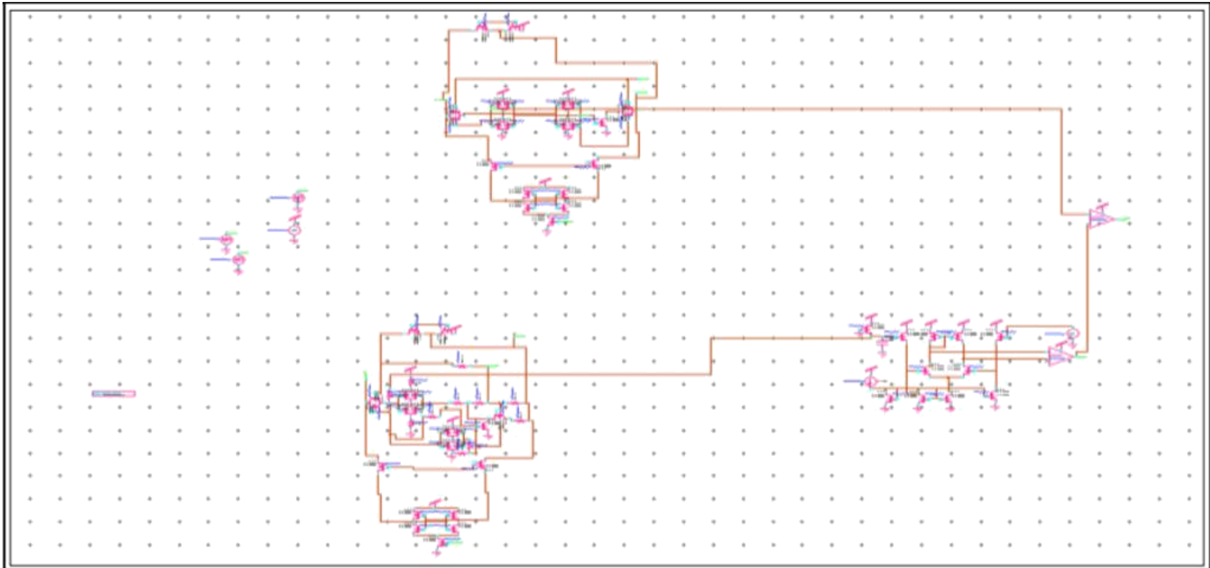

Figure 10: Schematic of BIST circuitry.

Figure 10 shows schematic of BIST circuitry.

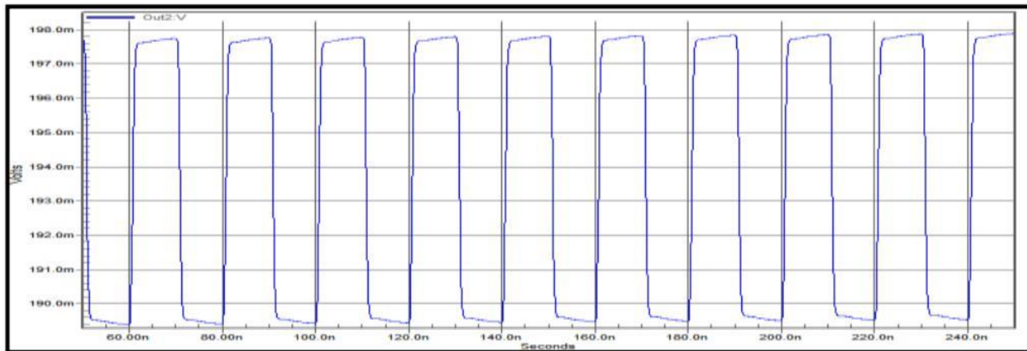

Figure 11: Fault detection using BIST circuitry.

Figure 11 shows that simulation result the data are written in circuit it can be read from sense amplifier through the 13T SRAM.

6T SRAM USING BIST (avg power in watts)	13T SRAM USING BIST (avg power in watts)
5.979 mW	1.793 mW

Table 2: SRAM using BIST.

Table 2 shows schematic of BIST circuitry.

Fault free SRAM (6T)	Fault free SRAM (13T)	Faulty SRAM (µA)(6T)	Resistor	Faulty SRAM (µA)(13T)
800 µA	150 µA	0.50	R1(1 MΩ)	0.25
800 µA	150 µA	0.10	R2(1 MΩ)	0.25
800 µA	150 µA	0.20	R3(1 MΩ)	0.50
800 µA	150 µA	0.60	R4(1 MΩ)	0.10
800 µA	150 µA	0.15	R5(10 Ω)	0.10
800 µA	150 µA	0.20	R6(10 Ω)	0.10
800 µA	150 µA	10.0	R7(10 Ω)	18.0

Table 3: Comparison table for different SRAM between power, delay, and noise.

Table 3 shows the comparison table for different SRAM between power, delay, and noise.

V. CONCLUSION

The Proposed BIST using transient current approach for fault detection is implemented and its effectiveness has been tested using simple memory architecture having single and multiple faults. Presence of fault is shown as a pulse in the output of the circuit. This BIST architecture may be extended to detect faults in larger SRAM array. A novel high performance BIST can be designed. High performance includes high speed, low power BIST.

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