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# VLSI Implementation and Area Efficient Cordic based Integer DCT Architectures for HEVC

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**ABSTRACT**:In signal progressing domain, recent days there is bottleneck parameter performance like area, latency. To provide area efficient integer Discrete Cosine Transform (DCT) designs for High Efficiency Video Coding (HEVC). So that invoked CORDIC architecture to produce on fly trigonometric output instead of traditional method. In integer DCT have its own style of operation and to calculate twiddle factor of DCT CORDIC architecture actively introduced and make sustainable result in area. The computational complexity has been reduced considerably half as compare to traditional operations. The Experimental result shows that the proposed Dct algorithm has not only reduces the computational complexity. Significantly, it also keeps the better transformation quality of the efficient integer DCT. Therefore, the proposed CORDIC based integer DCT can be used in area efficient and high speed HEVC systems especially in battery-based systems. The design has been verified using Modelsim 6.4se and obtain RTL schematic using Xilinx 13.1 Ise.

**KEYWORDs:** Discrete Cosine Transform (DCT), H.265, High Efficiency Video Coding (HEVC), Integer Discrete Cosine Transform (IDCT), CORDIC algorithm.

## I. INTRODUCTION

The critical normal for HEVC is that it chains DCT of distinctive sizes, for example, 4, 8, 16, and 32. In this way, the equipment building design ought to be sufficiently adaptable for the processing of DCT of any of these diverse lengths. The current outlines for customary DCT based on the constant matrix multiplication (CMM) and multiple constant multiplications (MCM) can give ideal answers for the processing of any of these distinctive lengths; however they are not reusable for any lengths to backing the same throughput transforming of Integer DCT of diverse change lengths. Considering this subject, this have broken down the conceivable usage of whole number DCT for HEVC in the situation of asset prerequisite and reusability and taking into account that, the proposed calculation has been inferred for equipment execution. This work has composed versatile and reusable architectures for 1-D and 2-D whole number DCTs for HEVC that could be reused for any of the endorsed lengths with the same throughput of handling regardless of change size.

Analyzing design with multiplication and its corresponding area results are not good to compare with current architectures. The current design invoking CORDIC based Integer DCT can be good to produce on fly computation of cosine terms instead of predefined stored values in LUT tables; this research has been completed on low power DCT designs. The most popular ways to detect the fast DCT (FDCT) and it can be used for Flow-Graph Algorithm (FGA) for VLSI-implementation.

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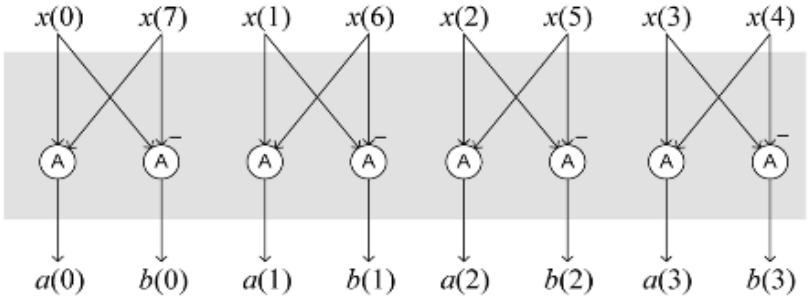
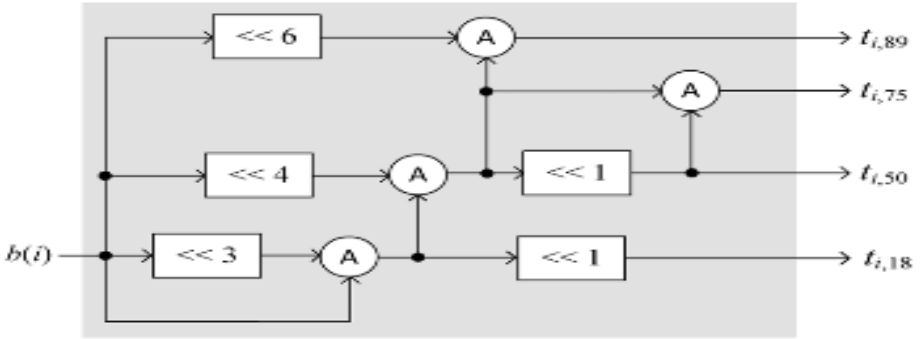
## II. TRADITIONAL ARCHITECTURE FOR EIGHT POINT INTERGER DCT

The Traditional architecture consists of three adder units. They are input adder unit (IAU), a shift-adder unit (SAU), and output adder unit (OAU). The calculation of t0, 64 and t1, 64 does not devour any rationale since the movement operations could be rewired in equipment. The structure of SAU is indicated given figure. Outputs of the SAU are at last added by the OAU as indicated by STAGE-3 of the calculation

### A) INPUT ADDER UNIT




### B) SHIFT-ADD UNIT




### C) OUTPUT ADDER UNIT

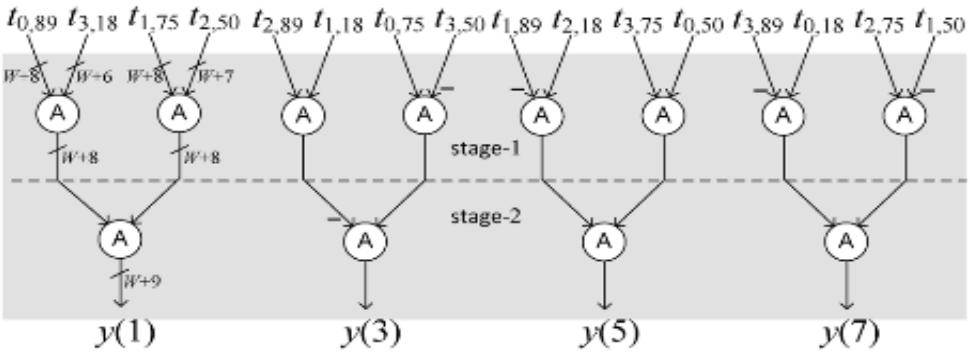



Fig 1.TRADITIONAL ARCHITECTURE FOR EIGHT-POINT INTEGER DCT

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## III. PROPOSED METHODOLOGY

The proposed outline has been summoning CORDIC based plan in an Integer DCT. This usage requires just 38 include and 16 movement operations. We have taken the first Integer DCT as the beginning stage for our improvement, on the grounds that the hypothetical lower bound of the quantity of increases needed for the 1-D 8-point DCT. Keeping in mind the end goal to infer the proposed calculation, we first consider the butterfly toward the start of diagram as demonstrated in Figure 2.

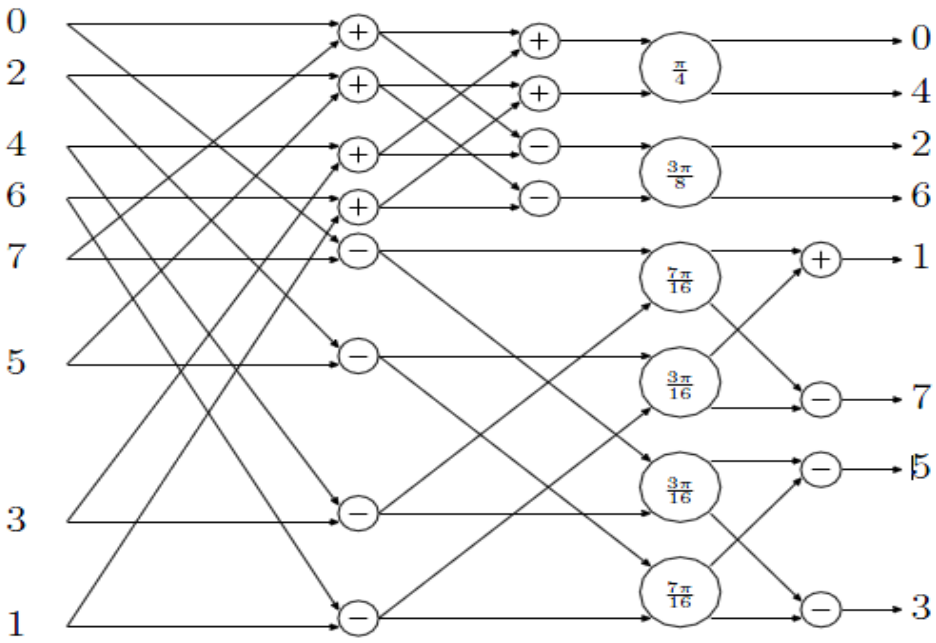


Fig 2.SIGNAL FLOW DIAGRAM OF INTEGER DCT WITH CORDIC

The degree butterflies with scaling variables 3pi/8, 1pi/16 and 3pi/16 can likewise be supplanted by CORDIC utilizing q = 3□ □ / 8, 1□ □ /16 and 3□ □ /16 separately. Henceforth, this can supplant all butterflies in the Integer DCT to determine the unadulterated CORDIC based Integer DCT. Next, the outline needs to decrease every turn edge and diminish the computational many-sided quality. Initial phase in this configuration is the extraordinary structure of the number DCT, toward the end of the stream chart for the edge q = pi/4. As such, the pi/4 pivot just needs two add operations to do the CORDIC turn. Second in this configuration for a point □ □ = 3□ □ / 8 it can be diminish the quantity of emphases to three furthermore move all repayment ventures to the outline. In spite of the fact that the improved 3□ □ / 8 revolutions will diminish the nature of the outcomes, the impacts are not clear in featurearrangement streams or picture pressure. Thirdly, when it investigate the point □ □ = □ □ /16, it can be effortlessly watched that the fancied count of the □ □ /16 turn is near to one. In this manner, it can overlook the figuring ventures of the □ □ /16 turn. Accordingly, it just wishes two emphases two iterations in the CORDIC computation.

## IV. PERFORMANCE EVALUATION

The Simulation Model is usually any VLSI design has been verified using simulation software and it is synthesized using implementation software. For a given input 4-point integer DCT has been verified.

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### A) Simulation Result of 8- point Integer DCT

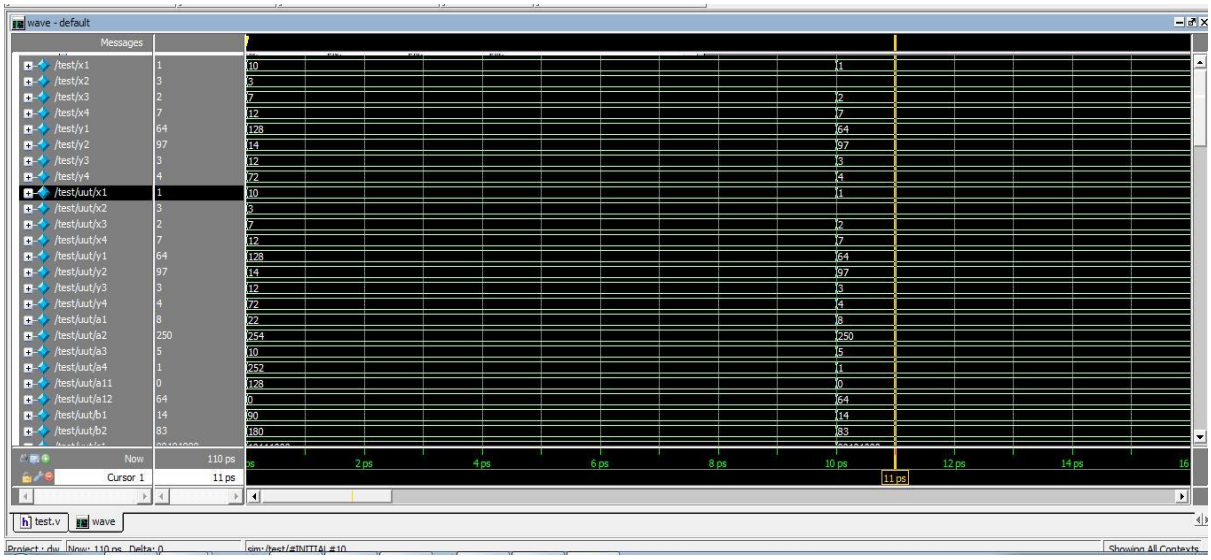


Fig 3.Simulation graph of 8-point integer DCT

### B) SYNTHESIS RESULT OF 8 – POINT EXISTING INTEGER DCT

The eight point integer DCT unit has been designed with CSA (Carry Select adder) and for multiplication operation left shifter has been used and it could perform multiplication operation where multiplication and addition operations are follows the algorithm, where multiplication have to perform at the same time where it have to do addition operation.Fig.4 Shows synthesis result of 8-point DCT with CSA.

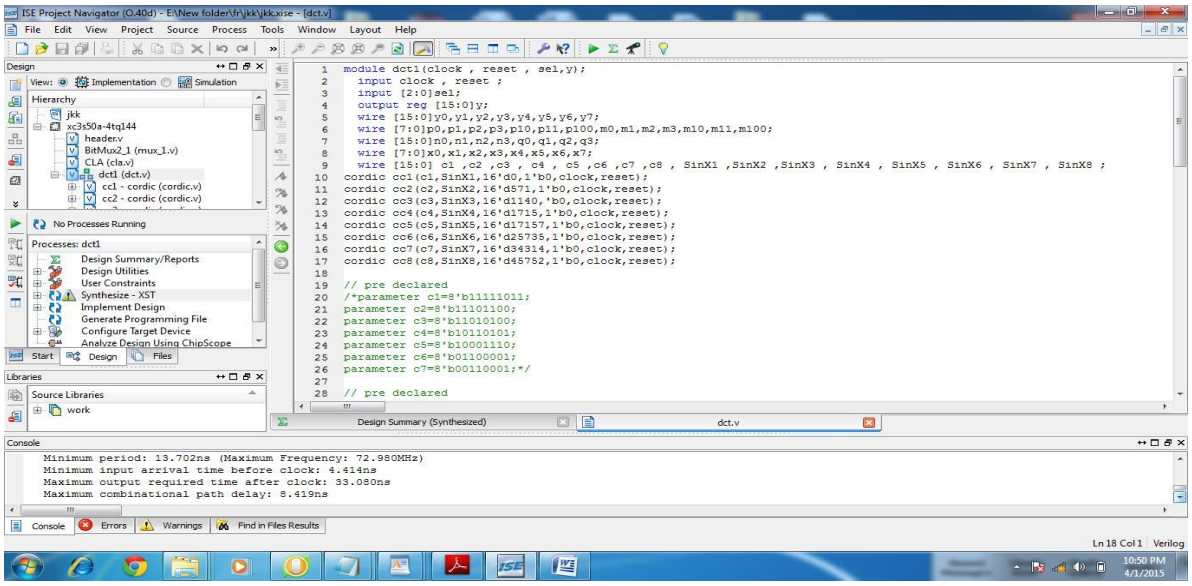


Fig 4. 8-point Existing integer DCT

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### C). SYNTHESIS RESULT OF 8 – POINT INTEGER DCT WITH CORDIC

The eight point integer DCT unit has been designed with CORDIC algorithm, to compute cosine terms in on fly need to compute Integer DCT, where multiplication have to perform at the same time where it have to do addition operation.Fig.5 Shows synthesis result of 8-point DCT with CORDIC.

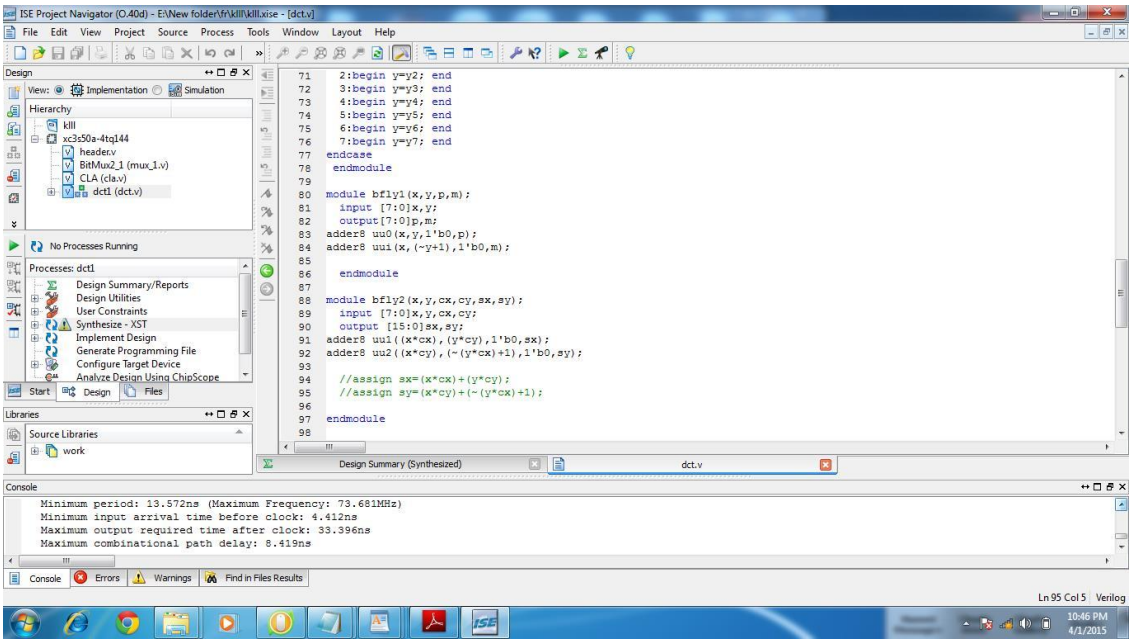


Fig.5 8-point integer DCT with CORDIC

**TABLE.1 COMPARISON BETWEEN CSA AND CLA OF 4-POINT DCT FOR SPARTAN 3E**

| Designs | Number of slices | Number of LUT's | Delay (ns) |
|---|---|---|---|
| Existing Integer DCT | 120 | 156 | 13.702 |
| Integer DCT with CORDIC | 78 | 110 | 13.52 |

The comparison results of existing and proposed design of 8-point Integer DCT with CORDIC having better parameter result as compare to CSA with 8-point DCT.

## V. CONCLUSION

In this paper, we propose a low tangling and awesome DCT change in light of the CORDIC computation is shown. The proposed CORDIC based Integer DCT building plan simply have need of 78 cuts rather than 120, number of LUT's are 110 rather than 156 and deferral has been diminished to .2ns so speed has been enhanced in ideal level. The proposed count not simply lessens the computational multifaceted design widely stood out from the first customary

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DCT; it in like manner keeps the considerable quality change result. In this look upon, the proposed DCT figuring is amazingly suitable for low zone and fast sign changing applications, for instance, HEVC.

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